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The variation of the leakage current characteristics of W/Ta_2O_5/W MIM capacitors with the thickness of the bottom W electrode

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ABSTRACT

In this paper, we will report that the leakage current characteristics can be a function of the bottom electrode. The variation of the bottom tungsten electrode thickness can affect the leakage current characteristics of W/Ta_2O_5/W MIM capacitors mainly through two mechanisms. The first mechanism is that the Ta_2O_5 CVD process can be influenced by the W bottom electrode thickness. Experimentally it was observed that the thickness of the Ta_2O_5 film deposited by CVD is noticeably different for samples with different bottom W electrodes with different thicknesses. The second mechanism is that the surface roughness of the bottom W electrode increases with increasing thickness, resulting in a smaller effective Schottky barrier height. A smaller effective Schottky barrier height will lead to larger leakage current.

1. Introduction

Metal-insulator-metal (MIM) capacitors are used in analog/mixed-signal CMOS integrated circuits [1,2]. For more advanced technology nodes, high-k dielectric materials have been used to replace traditional dielectric materials like SiO_2 or Si_3N_4 [3–5]. If the leakage current is low, it is possible to use a thinner high-k dielectric film, resulting in a larger capacitance density. In addition, MIM structures have also been investigated for RRAM (resistive random access memory) applications [6–8]. For the applications discussed above, the leakage current versus voltage (I–V) characteristics can be important. However, the underlying physics governing the I–V characteristics of thin film MIM capacitors involving high-k dielectric is still not well understood. Thus there is a practical need to understand the leakage current characteristics of MIM capacitors in greater depth.

In this paper, we will focus our attention on Ta_2O_5 deposited by chemical vapor deposition (CVD) as the dielectric material for MIM capacitors because it is a well proven high-k dielectric material technology [9]. Ta_2O_5 has a relative dielectric constant of ~20–25, compared to ~4 for SiO_2 [10–12]. MIM capacitors based on Ta_2O_5 or other high-k dielectric materials tend to show up an asymmetric current–voltage (I–V) characteristics even though the top and bottom electrodes are made of the same kind of metal for an apparently symmetric structure. In addition, when the thickness of the bottom metal electrode changes, the I–V characteristics can also change.

2. Experimental

In our work, tantalum oxide (Ta_2O_5) was deposited by CVD onto bare (100) Si wafers or W coated (100) Si wafers in a manner similar to the work by McKinley and Sandler [9]; W coating was done by sputtering. Tantalum ethoxide with the chemical formula of $Ta(OC_2H_5)_5$ was used as precursor with oxygen (O_2) serving as the oxidizing agent. Then tungsten (W) was sputtered onto the top of the Ta_2O_5 film again through a metal shadow mask to form the top metal contact. There might be "plasma damage" due to the sputtering process; post-metallization annealing (PMA) was done in nitrogen at 400 °C after W sputtering. Ta_2O_5 capacitors were electrically characterized using the Agilent B1500A Semiconductor Device Analyzer for I-V measurements.

Atomic force microscopy (AFM) was used to measure surface roughness of the W film after W sputtering onto Si wafers. Similarly, AFM was done on the top surface of the Ta_2O_5 film after CVD. Cross-sectional transmission electron microscopy (XTEM) was also performed to study interfacial roughness. XTEM samples were prepared by the Focused Ion Beam (FIB) technique. To protect the top surface of the Ta_2O_5 film, we deposited an Al film onto the top of the Ta_2O_5 film before FIB. Al was used because it is more transparent to electrons than tantalum oxide or tungsten during the performance of transmission electron microscopy. If tungsten is used as the top protective layer, tantalum oxide spikes can be very difficult to detect. The cross-section of the Al/

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Ta_2O_5/W/Si structure after FIB was studied by a transmission electron microscope (TEM).

3. Results and discussion

The thicknesses of the Ta_2O_5 films and the bottom W electrodes for 3 samples measured by XTEM are shown in Table 1. Ta_2O_5 films were deposited simultaneously for the 3 samples by CVD, and the thicknesses were meant to be 80 nm. However, the experimental results appeared to be different from the expected results. The surface roughness of a metal film varies with the film thickness, as shown in Fig. 1 [13]. All practical metal films used in microelectronics are in stage (c). They are polycrystalline and relatively rough. Practical metal films used in the microelectronics industry tend to be rougher when the metal film is thicker. Fig. 2 shows that the surface roughness (measured by atomic force microscope, AFM) of the bottom W electrode increases with increasing thickness. The easiest way to reduce the roughness of the W bottom electrode is to use a thinner W film for the bottom electrode. However, the thickness of the W bottom electrode should not be reduced to the ultra-thin regime (<10 nm) because the metal film may become "discontinuous".

Liu et al. pointed out that the deposition rate of CVD Ta_2O_5 was significantly higher on "relatively rough" rugged PtO than on Pt [14]. The effective deposition rate of CVD can be influenced by the presence of an "incubation time" due to the initial nucleation process according to Kajikawa et al. [15]. "Incubation time" is also known as "nucleation delay".

It is obvious that the incubation time for different substrates is different. So, it is expected that the incubation time is longer for a smooth surface than for a rough surface and that the incubation time can be made shorter by using a thicker metal film as substrate because a thicker metal film tends to be rougher. Thus it is expected that the incubation time for a smooth Si substrate is significantly larger than that for a rough W on Si substrate. Furthermore, the incubation time for a thinner W on Si substrate is larger than that for a thicker W on Si substrate. In other words, the thickness of the bottom W electrode can influence the nucleation characteristics of Ta_2O_5 CVD process.

Previously, Lau et al. pointed out that CVD has a surface smoothing effect such that the interface between the top metal and Ta_2O_5 tends to be smoother than the interface between the bottom metal and Ta_2O_5, resulting in a larger effective Schottky barrier height for the top interface and a smaller effective Schottky barrier height for the bottom interface [13]. Fig. 2 also shows the same result that the surface roughness of W bottom electrode is significantly reduced by the CVD process of Ta_2O_5 layer. Furthermore, XTEM picture of a Ta_2O_5/W/Si structure verifies the result that the top interface tends to be smoother than the bottom interface, as shown in Fig. 3. Therefore it is easy to figure out that a change in Ta_2O_5 thickness because of a change in "incubation time" can have a significant effect on the leakage current vs. voltage (I–V) characteristics of W/Ta_2O_5/W capacitors.

Fig. 4 shows electrical measurement results of W/Ta_2O_5/W capacitors. PMA means post metallization annealing. It is a necessary process for sample preparation to reduce the influence of sputtering for top electrode deposition. Plus ("+") means top electrode is biased positively, and minus ("−") means that top electrode is biased negatively. The voltage is applied with a step of 0.1 V. The logarithm of leakage current

Table 1
Bottom electrode (W) and Ta_2O_5 thickness of several samples measured by XTEM.

Sample name	Bottom W thickness (nm)	Ta_2O_5 thickness (nm)
Wafer 19	NA	70.2
Wafer 21	19.0	93.3
Wafer 23	92.5	97.8

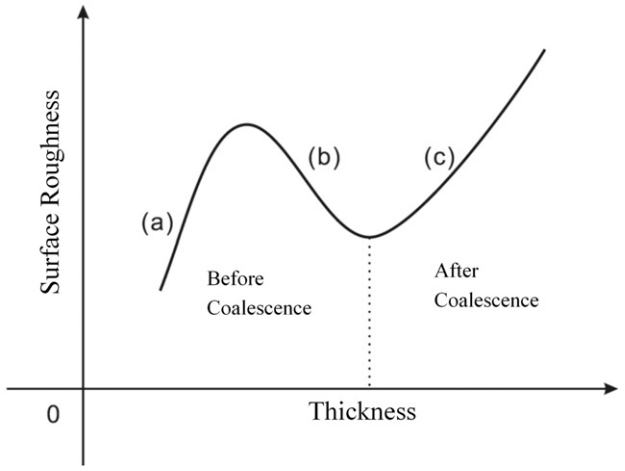

Fig. 1. The surface roughness of a metal film as a function of its thickness.

is plotted against the square root of voltage ($\sqrt{V}$) for Fig. 4(a) and the square root of electric field ($\sqrt{E}$) for Fig. 4(b), respectively.

When the top W is biased negatively, the leakage current of W23 appears to be smaller than that of W21, as shown in Fig. 4(a). This is because the Ta_2O_5 film of W23 becomes thicker because of the thicker bottom W film. Fig. 4(b) shows that the leakage current of W23 appears to be the same as that of W21 when the horizontal axis is the square root of the electric field instead of the voltage. When the top W is biased positively, the leakage current of W23 appears to be larger than that of W21, as shown in Fig. 4(a). This is because the effective Schottky barrier height between the bottom W and Ta_2O_5 becomes smaller because of the thicker bottom W film. The same conclusion can be reached as shown in Fig. 4(b). The difference between Fig. 4(a) and (b) can be noticed. However, it may be "marginal". The approach used in the present version of our paper is the more physically reasonable explanation.

The leakage current in a dielectric film can arise from several different conduction mechanisms including Schottky emission, Poole–Frenkel emission, Fowler–Nordheim tunneling, and space charge limited current. The current density due to Schottkey emission can be expressed as follows:

$$J \propto T^2 \exp\left[\frac{q\left(-\Phi_B + \sqrt{qE/4\pi\epsilon_i}\right)}{kT}\right] \quad (1)$$

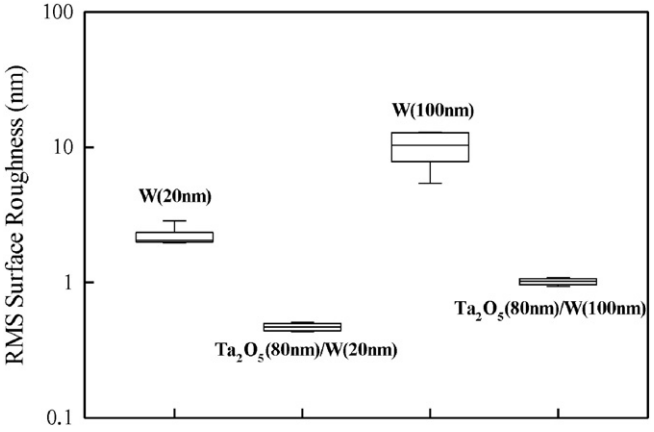

Fig. 2. RMS surface roughness of several samples measured by AFM showing the surface smoothing effect of CVD.