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Low-voltage linear silicon optical modulator with a single-drive parallel-push–pull scheme

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ABSTRACT

We demonstrate a single-drive parallel-push–pull silicon optical modulator. Compared with the serial-push–pull scheme, the parallel-push–pull scheme allows the driving signal to be applied on both the arms without division. It makes the device suitable for low-voltage driving. Since the electrode drives two PN junctions at the same time, we dope the waveguides periodically in order to lower the capacitance per unit length of the loaded PN junction. This design could alleviate the matching requirement of the coplanar waveguide electrode. When optically biased at the quadrature point, the device has an extinction ratio of 3.1 dB at the speed of 20 Gbps and under the driving voltage of 1.8 Vpp. Benefitting from the push–pull scheme, its linearity performance is also improved. Compared with the device adopting the scheme with only one arm being driven, the spurious free dynamic ranges for second-order harmonic distortion and third-order intermodulation distortion increase by 11.5 dB and 2 dB to 101 dB.$Hz^{1/2}$ and 113 dB.$Hz^{2/3}$, respectively.

1. Introduction

Silicon photonics has been intensively investigated by worldwide researchers for the last decades. It is regarded as a promising technology in many fields [1–14], especially in optical interconnect. Related product has been demonstrated by Intel Corporation recently [15]. Among the silicon photonic devices, silicon optical modulator is a key element in silicon optical link [16–20]. Normally it consumes most power budget of the silicon optical link due to its high driving voltage. In analog optical communication, the high linearity performance is a basic requirement. However, due to the carrier dispersion effect and the depletion mechanism of the PN junction, it is hard to achieve a comparable linearity performance as the commercial $LiNO_3$ optical modulator does [21–23].

Push–pull scheme is considered as a way to reduce the driving voltage and improve the linearity performance of the silicon Mach–Zehnder (M–Z) optical modulator [23].

Double-drive push–pull scheme, using a differential electrical signal to drive both the arms of the silicon M–Z optical modulator simultaneously, is a primitive way to realize the push–pull scheme. However, the time delay between the two electrical signals applied to the two arms becomes serious when the modulation speed is high.

The single-drive push–pull scheme, using a single electrical signal to drive both the arms of the silicon M–Z optical modulator, is an effective way to avoid the time delay problem [20,23]. With respect to the single-drive serial-push–pull scheme, the PN junctions embedded in the two arms are connected in series and the driving voltage is partially applied to each arm [20,23].

In this paper, we demonstrate a silicon M–Z optical modulator with single-drive parallel-push–pull scheme, in which two PN junctions are parallelly connected to the coplanar waveguide (CPW) electrode. The driving voltage is applied to both the two PN junctions without division, and then the driving voltage is lowered compared with the single-drive push–pull scheme. The phase shifter is periodically doped to make sure that the velocity of the electrical signal in the CPW electrode and the optical signal in the silicon waveguide are matched at a cost of footprint. The periodically doped waveguide also lowers the CPW electrodes' capacitance per unit length and increases the characteristic impedance. The device has an extinction ratio of 3.1 dB at the speed of 20 Gbps under a driving voltage of 1.8 Vpp when it is optically biased at the quadrature point. Compared with the device adopting the scheme with only one arm being driven, its linearity performance is also improved. The spurious free dynamic ranges (SFDR) for second-order harmonic distortion (SHD) and third-order intermodulation distortion (TID) are

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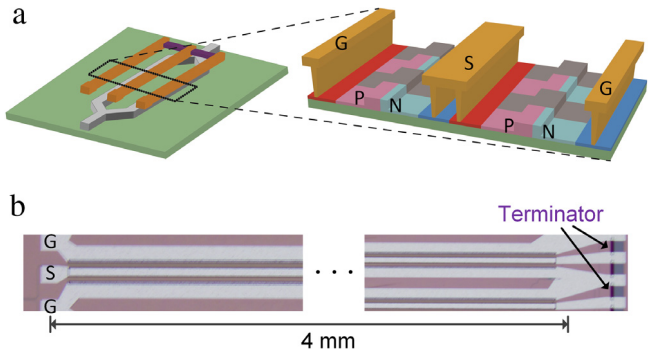

Fig. 1. (a) Illustration of the single-drive parallelly-push–pull scheme; (b) Microscope image of the fabricated device.

101 dB $Hz^{1/2}$ and 113 dB $Hz^{2/3}$, respectively. The performances make it suitable for applications in the optical interconnect and the analog optical communication when they are not critical of footprint

2. Design and fabrication

The device is schematically shown in Fig. 1(a), which is based on a M–Z interferometer. The electrode uses a pattern of ground-signal-ground (G-S-G) and is designed to be a CPW electrode. Two PN junctions are embedded in the two arms and parallelly connected to the S electrode. The relative positions of the two PN junctions are shown in Fig. 1(a). When a certain voltage is applied to the S electrode, one PN junction will be forward driven and the other will be backward driven to form a push–pull scheme. As the electrode is designed to drive the two arms at the same time, the loaded CPW electrode will have a large distributed capacitance, which will lead to a serious mismatch of the CPW electrode. The characteristic impedance of the CPW electrode will be much lower than 50 Ω and the group velocity will be reduced too. In order to overcome this problem, the phase shifter is periodically doped with a period of 20 μm. Half of the waveguide in one period is doped and the left half is not. As the shortest wavelength of the electrical signal is much larger than the doping period, this doping profile is supposed to reduce the capacitance per unit length of the PN junction and make a good match of the CPW electrode especially for the characteristic impedance and the group velocity of the electrical signal. At the other end of the CPW electrode, the terminators are integrated to absorb the transmitted electrical wave to avoid the reflection of the electrical signal.

We utilize the silicon photonics foundry of Institute of Microelectronics in Singapore for device fabrication. The 8-inch silicon-on-insulator wafer with a 220 nm top silicon layer and a 3 μm buried oxide is adopted to fabricate the device. 248 nm deep ultraviolet photolithography is used to define the patterns. All the fabrication process is compatible with the complementary metal oxide semiconductor (CMOS) process. The ridge waveguide has a width of 400 nm, a height of 220 nm and a slab thickness of 70 nm. The PN junction is to the right of the middle of the silicon optical waveguide with an offset of 40 nm so that the p-type depletion region has a largest overlap with the strongest optical power region. Therefore the device has a maximum modulation efficiency. The p-doping concentration is $1\times10^{18}/cm^3$ and the n-doping concentration is $8\times10^{17}/cm^3$. Fig. 1(b) shows the micrograph of the silicon optical modulator based on an asymmetric M–Z interferometer. Titanium nitride resistors as the terminator are integrated on the chip. The periodically doped phase shifter is 4 mm in length and only half of it is doped. The width of the MMI is 6 μm, and the length is 32 μm. The signal metal has a width of 30 μm and a gap of 11.5 μm with the ground metal.

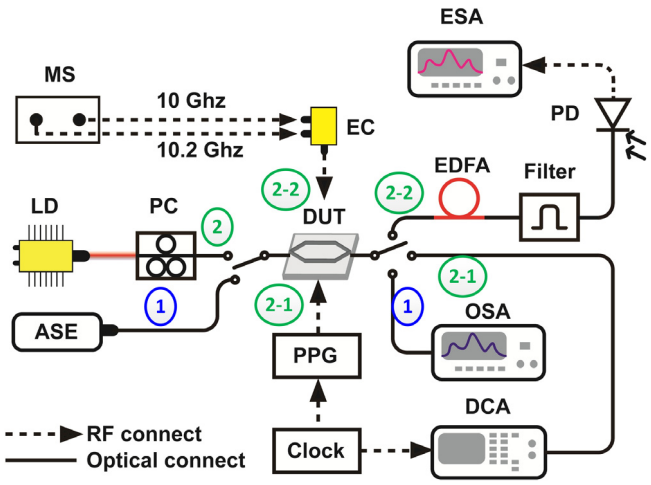

Fig. 2. Experimental setup for the digital signal modulation and linearity performance characterization. LD: laser diode; PC: polarization controller; ASE: amplified spontaneous emission; PPG: pulse pattern generator; DCA: digital communication analyzer; OSA: optical spectrum analyzer; EDFA: erbium-doped fiber amplifier; PD: photodiode; ESA: electrical spectral analyzer; EC: electrical combiner; MS: microwave source.

3. Experiments and discussion

Fig. 2 schematically shows the experimental setup for the digital signal modulation and linearity characterization. Link 1 is used to characterize the spectral response of the device. Link 2 has two sub-links. Link 2-1 is used for the digital signal modulation experiment. Link 2-2 is used to characterize the linearity performance of the device. Firstly, continuous-wave (CW) light from a laser diode is controlled by a polarization controller (PC) and then coupled into the device through a lensed fiber. The PC is used to guarantee that the polarization of the CW light is consistent with the TE polarization of the silicon waveguide as it only supports the fundamental quasi-TE mode. The coupling loss of the device is about 2.5 dB/facet. The on-chip insertion loss of the device is about 3.8 dB, which includes the propagation loss of the phase shifter (3.2 dB) and the propagation loss of two MMI couplers (2×0.3 dB). The modulated optical signal is directly fed into an optical spectral analyzer to observe the spectral shift and measure the modulation efficiency.

A device without the terminator is specially fabricated to measure the modulation efficiency since the heat from the terminator can obviously affect the result. The measured modulation efficiency is shown in Fig. 3. As the applied reverse voltage increases, the modulation efficiency will decrease because the depletion width increment of the PN junction becomes smaller as the voltage increases. The relationship between the modulation efficiency and the applied reverse voltage roughly follows a square root function. Fig. 3 shows that the fitted line matches the experimental result well. Additionally, the measured low modulation efficiency in Fig. 3 is caused by the periodic doping. Actually half of the phase shifter is not doped and has no contribution to the modulation efficiency. If we fix the insertion loss and compare with the results in literatures [17–19], $V_{\pi L}$ number shall be divided by two. From Fig. 3, we find that the device operated around zero bias has a maximum modulation efficiency and is suitable for low driving operation. Therefore, both the two PN junctions in the two arms have no reverse biases when the device works dynamically.

Fig. 4 shows the electro-optical responses. The back curve shows the response of the single-drive parallel-push–pull device and The 3 dB bandwidth is 12.4 GHz. The blue curve shows the response of a normal device where one CPW electrode only drives one arm and is loaded by one PN junction [19]. The length of the doped silicon waveguide is 2 mm and all the doped 2 mm silicon waveguide is fully doped without periodic doping. The bandwidth is 18.4 GHz. Both the devices are electrically biased at 0 V. The reduction of the bandwidth is a