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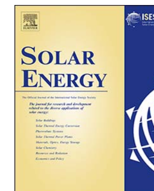

Development of *in-situ* high-voltage and high-temperature stressing capability on atomic force microscopy platform

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ABSTRACT

Reliability has become an increasingly important issue as photovoltaic technologies mature. However, researching reliability at the nanometer scale is in its infancy; in particular, *in-situ* studies have not been reported to date. Here, to investigate potential-induced degradation (PID) of solar cell modules, we have developed an *in-situ* stressing capability with applied high voltage (HV) and high temperature (HT) on an atomic force microscopy (AFM) platform. We designed a sample holder to simultaneously accommodate 1000-V HV and 200 °C HT stressing. Three technical challenges have been overcome along with the development: thermal drift at HT, HV interference with measurement, and arc discharge caused by HV. We demonstrated no observable measurement artifact under the stress conditions. Based on our *in-situ* stressing AFM, Kelvin probe force microscopy potential imaging revealed the evolution of electrical potential across the junction along with the PID stressing time, which provides vital information to further study the PID mechanism.

1. Introduction

The global photovoltaics (PV) market and installed PV capacity have grown rapidly over the past decade through a combination of PV technology advances and policy initiatives (Haegel et al., 2017). In step with this growth, PV performance reliability has become increasingly important. Among all the reliability issues, potential-induced degradation (PID) has received extensive attention because it can lead to a massive decrease of module performance (Luo et al., 2017; Hacke et al., 2010a, 2010b; Pingel et al., 2010; Berghold et al., 2010). PID is due to the potential difference between the module frame/glass and solar cell. This effect occurs in all major types of solar modules and becomes more severe with an increase of solar array system voltage. Currently, extensive study of PID is at the panel/cell scale (Hacke et al., 2010a, 2010b; Pingel et al., 2010; Berghold et al., 2010; Hacke et al., 2013, 2014); however, this effect has only been studied by limited microscopy characterization methods (Harvey et al., 2016; Naumann et al., 2013, 2014; Johnston et al., 2016), such as secondary-ion mass spectrometry and transmission electron microscopy. These measurements can provide a deeper understanding of PID-related defect chemistry and structure, and electrical properties of the p-n junction. However, these powerful analytical tools only examine a certain degree of degradation, and the PID mechanism remains unclear. Questions related to the fundamental mechanism such as sodium contamination and partial recovery have yet to be answered (Luo et al., 2017). It is has been well reported that Na diffuse into stacking faults and cause the local shunting of p-n junction. However, it is not clear whether the stacking faults existed before the PID or were induced by the PID. Moreover, it is questionable whether the local shunting is the only PID mechanism. PID can be reversible and metastable, so *in-situ* monitoring of microscopic structural, electrical, and opto-electrical changes under stresses allows direct observation of degradation kinetics and reveals transitions of reliability-related metastable states. Such observation may be impossible in *ex-situ* studies, and the *in-situ* monitoring provides the possibility to gain a deeper understanding of the PID mechanism.

Atomic force microscopy (AFM)-based characterizations have been unique and powerful tools to study nanometer (nm)-scale electrical properties of solar cells (Xiao et al., 2015, 2016, 2017; Li et al., 2017; Wang et al., 2017; Jiang et al., 2012, 2013, 2008; Ke et al., 2016). Here, we have developed an *in-situ* stressing capability based on our AFM platform: a sample holder is designed to stress a small piece of solar module (1 cm × 1 cm) at high voltage (HV) up to 1000 V and

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simultaneously at high temperature (HT) up to 200 °C. The accelerated life test (ALT) standard condition for PID is 1000 V at 85 °C (Luo et al., 2017; Harvey et al., 2016). This experimental design and setup allowed us to do ALT and measure the change in nm-scale electrical properties with degradation in real time. Specifically, we apply Kelvin probe force microscopy (KPFM) measurements on cross-sections of the devices, with direct imaging of the evolution of the electrical potential across the junction with nm resolution during the degradation process. In this paper, we will show thermal-drift suppression under different high temperatures, KPFM test results with and without the HV and HT stresses, as well as preliminary *in-situ* HV stressing results of potential images across a multicrystalline silicon (mc-Si) junction along with the degradation process. In addition to KPFM, the *in-situ* stressing capability on the AFM platform can also be used for other nanoelectrical probes such as scanning capacitance microscopy (SCM) (Jiang et al., 2012), scanning capacitance spectroscopy (SCS) (Xiao et al., 2017), scanning spreading resistance microscopy (SSRM) (Jiang et al., 2013), and conductive AFM (Ke et al., 2016).

2. Experimental

2.1. Experimental design and technical barrier

We designed and tested a sample holder based on our existing AFM platforms, to accommodate two stressing capabilities of 0–1000-V HV and 25–200 °C HT. The design SOLIDWORKS files are shown in supporting materials (Figs. S1–9). Fig. 1 shows a photo of the designed sample holder that is capable of simultaneous HV and HT stressing and is compatible with all the electrical imaging of KPFM, SCM, SCS, SSRM, and conductive AFM. Fig. 2 schematically shows functions of the sample holder. A piece of sample of an mc-Si solar cell module is subjected to the HV and HT stressing, while the nm-scale electrical imaging on cross-sections of the sample is being performed with a bias voltage applied to the cell, in order to image the electrical change across the junction. Three key challenges that our development confronted and has overcome are the following: thermal drift, HV interference with the electrical measurement, and HV arc discharge. Thermal drift is detrimental for high-resolution microscopy study, and the drift becomes more serious as temperature increases. As HV is applied across the solar module glass, electric field leakage can substantially interfere with the small potential (~1 V) measurement across the solar cell junction. Because the AFM-based techniques use small (centimeter-size) samples, the HV can cause arc discharge that may damage the sample and apparatus.

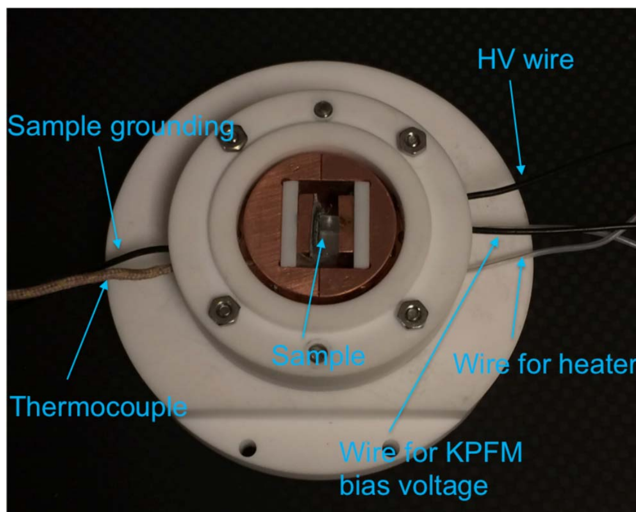

Fig. 1. A photograph of the *in-situ* stressing sample holder based on the AFM platforms.

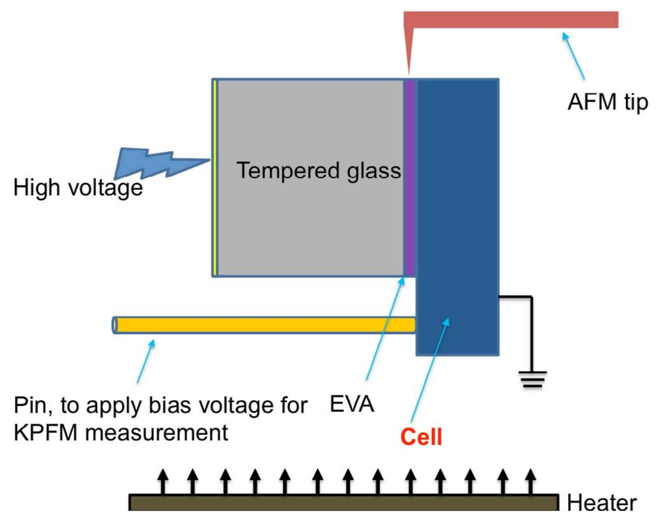

Fig. 2. A schematic illustrating functions of the sample holder with a high voltage applied to the module glass, a low voltage applied across the solar cell junction, and a ceramic resistance heater.

2.2. Cross sectional sample preparation

To simulate the PID process, the sample structure is made to be identical to a silicon module: a piece of mc-Si cell is covered by pre-polymerized ethylene vinyl acetate (EVA) and a tempered solar glass. The silicon solar cell studied in this work is the conventional Boron-doped p-type Si, with a single front junction (Phosphor-doped emitter) and SiN_x on top. The working solar cell (shunt resistance larger than 500 ohm-cm^2) was partially covered by the glass (as shown in Fig. 2) to expose the cell's front contact so that a bias voltage can be applied across the cell; this procedure is needed for the KPFM measurements to avoid the effect of the fixed surface charge (Jiang et al., 2008). In other electrical measurements of SCM and SSRM, a bias voltage is applied to the whole cell through either the front or back contacts but not across the cell, so the cell is not required to be alive (sufficiently large shunt resistance). Because the AFM-based imaging technique requires a flat surface, the sample was fine-polished to make the overall corrugation of the cross-section surface less than 20 nm. The polishing procedure was chemical-mechanically polishing with deionized water using a set of different diamond pads with particle size down to 100 nm, and followed by a polishing using silica colloids with a soft cloth (Jiang et al., 2008). Note that the tempered glass, EVA, and silicon cross-sectional surface need to be in the same plane for cross-sections of the different materials to be polished to the same height. As a result, the polishing needs to be for more than ~2 h and must be constantly checked to make sure the soft EVA material will not cover the front side of the silicon solar cell.

3. Results and discussions

3.1. Thermal drift suppression

Thermal drift occurs when there is heat exchange with the surrounding environment. The sample holder and the sample are made of different materials and have complicated geometries. So any small mismatch of thermal expansions can cause huge thermal drift in the nm to µm scales. In practice, it takes a very long time to reach a true thermal equilibrium state when there is a significant temperature difference between the material and surrounding environment. Even though the temperature measured by a thermocouple stabilizes within a fraction of a degree, a small thermal change can still cause significant thermal drift at elevated temperatures. We designed the sample holder with two approaches to suppress thermal drift of the sample: (1) make

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