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Line-impedance matching and signal conditioning capabilities for high-speed feed-forward voltage-mode transmit drivers

Khaldoon Abugharbieh [a,*], Abraham Balabanyan [b], Armen Durgaryan [b], Vazgen Melikyan [b]

[a] Electrical Engineering Department, Princess Sumaya University for Technology, Amman 11941, Jordan
[b] Synopsys Armenia CJSC, Yerevan, Armenia

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ABSTRACT

This work presents the design and implementation of a power-efficient 2-tap feed-forward voltage mode driver which has impedance tuning and signal conditioning capabilities. The driver has a robust mechanism to match its impedance to the line impedance even when signal conditioning is enabled which minimizes reflection and improves signal quality. A mixed signal approach that detects and compensates for NMOS and PMOS transistor resistance variation is presented. An analog circuit detects the driver's resistance variation, and a digital circuit controls an analog compensation circuit to maintain line impedance matching for all signal conditioning configurations of the driver. When maximum signal conditioning is enabled, the driver can transmit a 40 Gbits/sec PRBS7 signal through a 10 in. FR4 channel. It achieves a differential eye-opening amplitude of 100 mVppd and an eye-opening width of 0.8 UI consuming 9.7 mW of at-speed power. Simulations demonstrate that worst case impedance deviation from 50 Ω due to process, voltage and temperature variation is 2.7%. The driver is designed in 28 nm CMOS process using a 0.85 V nominal supply voltage. It is simulated using HSPICE circuit simulator and mixed mode simulations tools.

1. Introduction

Serial data communications systems have been coming increasingly common due to the high cost and synchronization difficulty of transferring parallel data. Fig. 1 shows a simplified serial data communications system where the parallel data is serialized in the transmitter and de-serailized in the receiver. Transmit and receive phase locked loops are used to synchronize data transfer. But, while serial data transfer is cost effective, the speed of the bit transfer rate is limited by the characteristics of the channel and the ability of the transmit driver and receiver to send and recover data. As data rates increase, transmitted signals are attenuated due to bandwidth limitations of the communications' channels. As a result, the binary data will spread into the adjacent symbols, which is known as intersymbol interference, or ISI, which has an adverse impact on Bit Error Rate (BER). To reduce the effect of ISI, the transmitted signal is given extra amplitude during transition which amounts to a signal boost in high frequency. This is a signal conditioning technique called feed-forward equalization, FFE. It can have a frequency characteristic like a high pass filter as shown in Fig.1.

Fig. 2 shows an example of a transmitter waveform that has a signal boost during switching. The duration of the boost is often set to one unit interval, because it is achieved by utilizing a delayed bit from the bit that is being transmitted. For optimal eye height and eye width at the receiver, the signal boost in the transmitter should match the loss in the channel at the data rate of interest. If the signal boost is less than the loss of the channel, the transmitted signal will be under equalized at the receiver. If the signal boost is greater than the loss of the channel, the transmitted signal will be over equalized. In addition to the high frequency signal boost, the transmitter impedance should be matched to the channel's impedance to achieve good return loss as predicted by Eq. (1) where Z_o is the single-ended impedance of the transmission channel and Z_{TX} is the differential impedance of the transmitter, [1]. To maintain acceptable signal integrity, signal reflection should be minimized as required by most modern communications' systems like DDR and USB [2]. Most communications channels have a characteristic impedance, Z_o, of 50 Ω.

$$\text{Return Loss}(dB) = 20 \log \left| \frac{2 \times Z_o + Z_{TX}}{2 \times Z_o - Z_{TX}} \right| \quad (1)$$

Common mode logic, CML, based transmitter topologies are still common in recent works [3–8], because transmitter impedance matching to 50 Ω is achieved using linear resistors. Furthermore, current steering techniques in the output stage are used to achieve signal conditioning capabilities. Fig. 3 shows a simplified schematic of a CML output stage. The output swing depends

* Corresponding author.
E-mail address: k.abugharbieh@psut.edu.jo (K. Abugharbieh).

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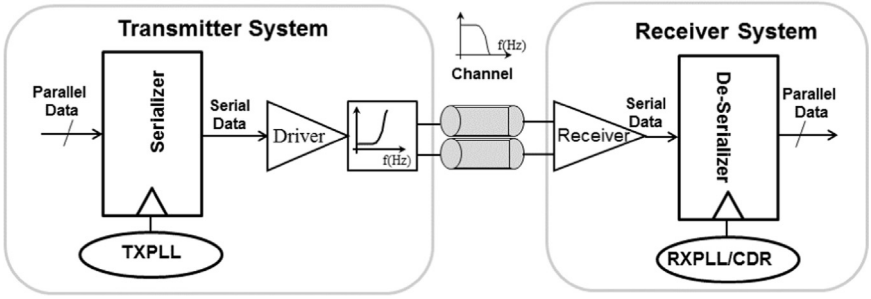

Fig. 1. Conceptual model of a serial data transfer system.

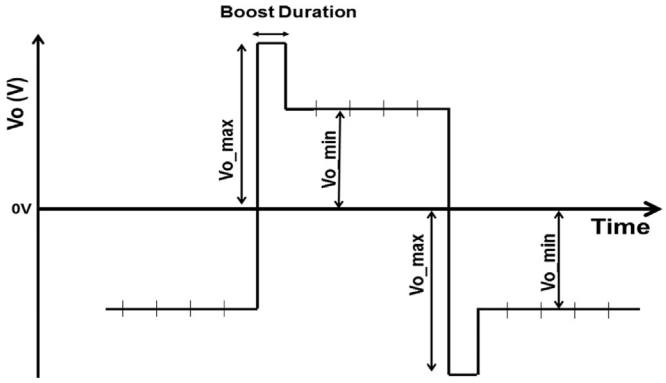

Fig. 2. A sample transmitter output voltage with high frequency boosting.

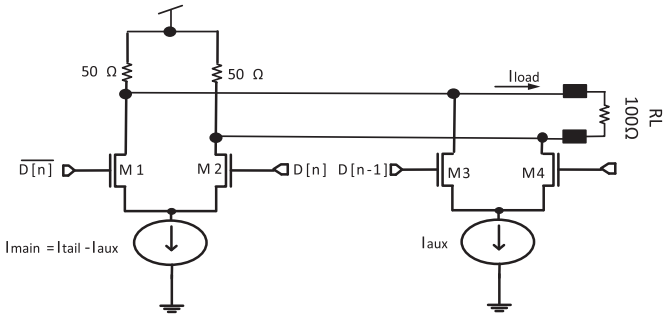

Fig. 3. Simple CML transmitter with signal conditioning.

Table 1
Current mode and voltage mode transmit drivers comparison.

	Power	Line impedance matching difficulty	Matching elements	Signal equalization mechanism
Voltage Mode Driver	Low	high	FETs	FETs' Impedance Configuration
Current Mode Driver	High	low-Medium	Linear Resistors	Current Steering

on the data pattern and is predicted by Eqs. (2) and (3) where R_L is the differential resistance of the transmission channel. For example, if the data is changing, like pattern 010, the amplitude swing is maximum as in Eq. (2). However, when the data is steady, like pattern 111, the amplitude swing is minimum as predicted by Eq. (3).

$$V_{o,\,cml\_\,max} = R_L \times I_{load\_\,max} = R_L \times \frac{I_{tail}}{4} \tag{2}$$

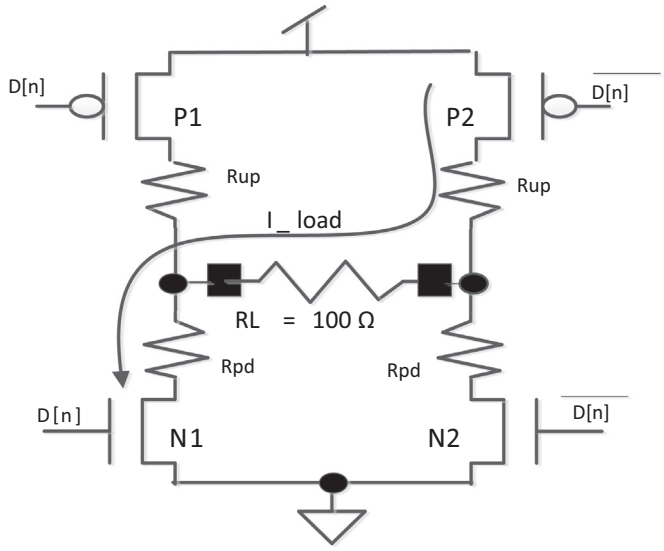

Fig. 4. Simplified conventional voltage mode transmitter.

$$V_{o,\,cml\_\,min} = R_L \times I_{load\_\,min} = R_L \times \left(\frac{I_{tail} - 2{*}I_{aux}}{4}\right) \tag{3}$$

While CML topologies are common, because matched transmitter impedance is achieved using linear poly resistors, they are not power efficient. As shown in Eqs. (2) and (3), the transmitter consumes a current that is proportional to four times the load current, I_{load}. Further, transistors M1-M4 need to have sizes that are large enough to fully switch the current between the two legs of the transmitter. This increases the drain to bulk and drain to gate parasitic capacitance which has adverse effects on high speed operation. Finally, CML based topologies become less competitive as modern technologies use lower supply voltages which causes headroom issues for the main and auxiliary tail current sources. As a result, voltage mode transmit drivers are becoming more popular [9–17]. However, it is challenging to match the impedance of a voltage-mode transmitter to the line impedance, because FETs, biased in the linear region, are used as matching elements. A FET can behave non-linearly and significantly changes its impedance across process, voltage and temperature, PVT, variations [18–20]. Further, achieving signal conditioning, FFE, is not as straight forward as it is in CML topologies, because it is done using the reconfiguration of the impedances of the FETs used. Table 1 summarizes the merits and demerits of both current mode and voltage mode transmit drivers.

In [14], a voltage mode driver is proposed that achieves 20 Gbps operation. But, passive high pass RC filters are used to achieve signal conditioning due to the absence of D[n−1] signal. In [15], a hybrid approach was presented where the main transmitter was a voltage mode driver, but the equalization was