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Improvement of crystallinity for poly-Si thin film by negative substrate bias at low temperature

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ABSTRACT

Polycrystalline silicon (p-Si) thin films are fabricated by plasma enhanced chemical vapor deposition (PECVD) at low substrate temperature (180 °C) with high-hydrogen dilution. Negative DC substrate bias is applied during the deposition process for improving the crystallinity of thin films. It is found that there is a phase transition from nanocrystalline phase to polycrystalline phase at negative bias = 50 V, as identified by scanning electron microscopy (SEM). The optimized p-Si thin film with large grains (~480 nm) are obtained at negative bias = 100 V. The deconvoluted Raman spectra reveal that the p-Si thin film is a mixture including amorphous silicon (a-Si), nanocrystalline silicon (nc-Si) and p-Si, and the crystalline volume fraction gradually increases with the substrate negative bias in the range of 0–100 V. The impacts of negative bias on the optical and electrical properties of p-Si thin films have been investigated. The growth mechanism of the p-Si grains has been discussed in detail. A grain-merging model is proposed for explaining the effect of negative bias on the formation of large p-Si grains at low temperature.

1. Introduction

As a useful material for possible application in electronic and optoelectronic devices, polycrystalline silicon has been studied for dozens of years [1–5]. Comparing with a-Si, p-Si material is superior in conductivity and carrier mobility [1]. The well crystallized p-Si thin film with thickness smaller than its grain size shows remarkable electrical properties comparative to those of single crystalline silicon wafer [2,3]. Due to the excellent characteristics, the p-Si thin films have been widely used in devices such as thin film transistors (TFT), image sensors, solar cells and active matrix organic light-emitting diode (AMOLED) [4–9].

Generally, conventional methods for obtaining p-Si thin film containing large crystalline grains include two steps: deposition of a-Si thin film and re-crystallization. In re-crystallization process, annealing is performed on the as-grown a-Si thin film for realizing nucleation and grain growth. Upon sufficient post-annealing treatment, p-Si grains may grow up to dozens of micrometers in size. Nowadays, various post-treatment approaches have been developed for re-crystallization, such as solid phase crystallization (SPC), excimer laser annealing (ELA), metal induced crystallization (MIC) and rapid thermal annealing (RTA) [10–13]. However, there are distinct disadvantages for these methods: (1) multi-step process is difficult to control, (2) substrate temperature in post-treatment is fairly high (>400 °C), beyond the capacity of a lot of substrate materials, (3) contamination is unavoidable in multi-step process, especially for the MIC. Due to these disadvantages, the application of p-Si is limited.

With the aim at manufacturing p-Si-based devices, low substrate temperature is required for satisfying the compatibility of substrate materials such as glass or plastic. Direct deposition methods, including PECVD and magnetron sputtering, are of advantage as p-Si thin film can directly grows on substrate without post-treatment [14–16]. However, the obtained p-Si grains have rather small size (<100 nm) in case of relatively low substrate temperature (≤300 °C). So it is necessary to develop a direct deposition technique for improving the grain size of p-Si thin film. In previous researches, appropriate negative DC substrate bias has been demonstrated to be beneficial for enhancing the crystallization of nc-Si [17]. It has been reported that the crystallization of nc-Si thin film is promoted by applying direct substrate bias to PECVD process while using He-diluted SiH_4 as precusor [18]. Similarly the degree of crystallinity has been identified to be improved under adequate negative substrate bias when using microwave (MW) CVD [19]. Fan et al. pointed out that negative bias can not only improve crystallinity but also decrease residual stress for nc-Si thin film [20]. According to these studies, negative substrate bias should be considered as an effective way for enhancing crystallization and improving grain size. In this work, the p-Si thin film with grain size of hundred nanometers has been fabricated by PECVD. During deposition, the negative bias was applied to substrate while the hydrogen dilution was set to a very high degree. The whole experiment proceeded at relatively low substrate

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temperature (180 °C) without post-treatment. The grow mechanism has been detailedly illustrated.

2. Experimental

The polycrystalline silicon thin films were prepared in a 13.56 MHz capacitively coupled plasma CVD system, no post-treatment was carried out. The electrode area was 133 cm^2 and the distance between parallel electrodes was 2 cm. Before experiments, the vacuum system was evacuated to 2.6×10^{-4} Pa. The substrate temperature was fixed at 180 °C during the deposition process while the RF power of 120 W was applied. The feed gas pure silane (SiH_4) was introduced into the chamber together with pure hydrogen (H_2), and a very high dilution ratio H_2/SiH_4 of 200/1 was used. The total chamber pressure was maintained at 400 Pa. During deposition, negative bias was applied on substrate and varied from 0 to 150 V.

In our experiments, corning 7059 glass was chosen as substrate and pre-cleaned by acetone, ethanol and deionized water in subsequence prior to deposition. The crystal structure of the thin films were analyzed by means of X-ray diffraction (XRD), an X-ray diffractometer (Siemens D5005) was applied in the 2θ range of 20–60°, the glancing-angle mode was used and the glancing angle is fixed at 1°, the thicknesses of samples are set to ~400 nm. A scanning electron microscope (SU8020) was employed to study the micro-morphology of the samples. The crystalline volume fraction (F_c) of the p-Si thin films was evaluated from Raman spectroscopy obtained from an in Via Reflex Raman spectrometer with a laser at 532 nm. The deposition rate of the thin films was estimated based on deposition time and thickness measured by a step profiler (Dektak 150). In order to directly observe the structure of the thin film, high-resolution transmission electron micrographs (HRTEM) images were obtained by means of a JEOL-JEM2100 transmission electron microscope operating at 200 kV, and the samples were deposited on carbon-coated copper grid for TEM observation. The transmittance spectra were measured by a UV-lambda 950 UV–visible spectrophotometer in the wavelength range of 300–1000 nm. The Hall measurement was carried out using a Nano-metrics HL5500PC system.

3. Results

Fig. 1 reveals the SEM surface morphologies of the films deposited with negative bias varying from 0 to 150 V. As seen in Fig. 1a, the as-grown film without negative bias is found to be composed of a large amount of irregular clusters which are amorphous-like in appearance, and there is no crystalline grain visible. For negative bias = 50 V, tiny and well separated grains with an average diameter of ~80 nm are clearly observed in Fig. 1b, indicating a phase transition under the effect of negative bias. As negative bias improves to 100 V, the average grain size grows dramatically and is estimated to be ~480 nm according to Fig. 1c. The huge grains are spherical in shape and have rough surface. Besides them, the amorphous-like clusters can also be observed. It suggests that the thin film deposited with negative bias applied to substrate may be a mixture of different components. The morphology of thin film deposited at 150 V is shown in Fig. 1d, the film surface appears similar to that shown in Fig. 1a and no grains are observed.

XRD spectra of the thin films deposited with negative bias varying from 0 to 150 V are shown in Fig. 2. Three individual diffraction peaks are observed, respectively corresponding to (111), (220) and (311) crystallographic planes of c-Si at 2θ of ~28.1°, 47.3° and 56.6°. Thereinto the prominent (111) peak and rather weak (311) peak are found for all the samples. The (220) peak exhibits significant enhancement as the negative bias increases from 0 V to 100 V, indicating the promoted preferred growth of (220) orientation. When the negative bias reaches 150 V, the (220) peak becomes weak again. The (111) plane of c-Si is the closest packed crystallographic plane originating from random nucleation with the lowest surface energy [21], and the (220) plane of the c-Si denotes the grain growth determined by thermodynamical

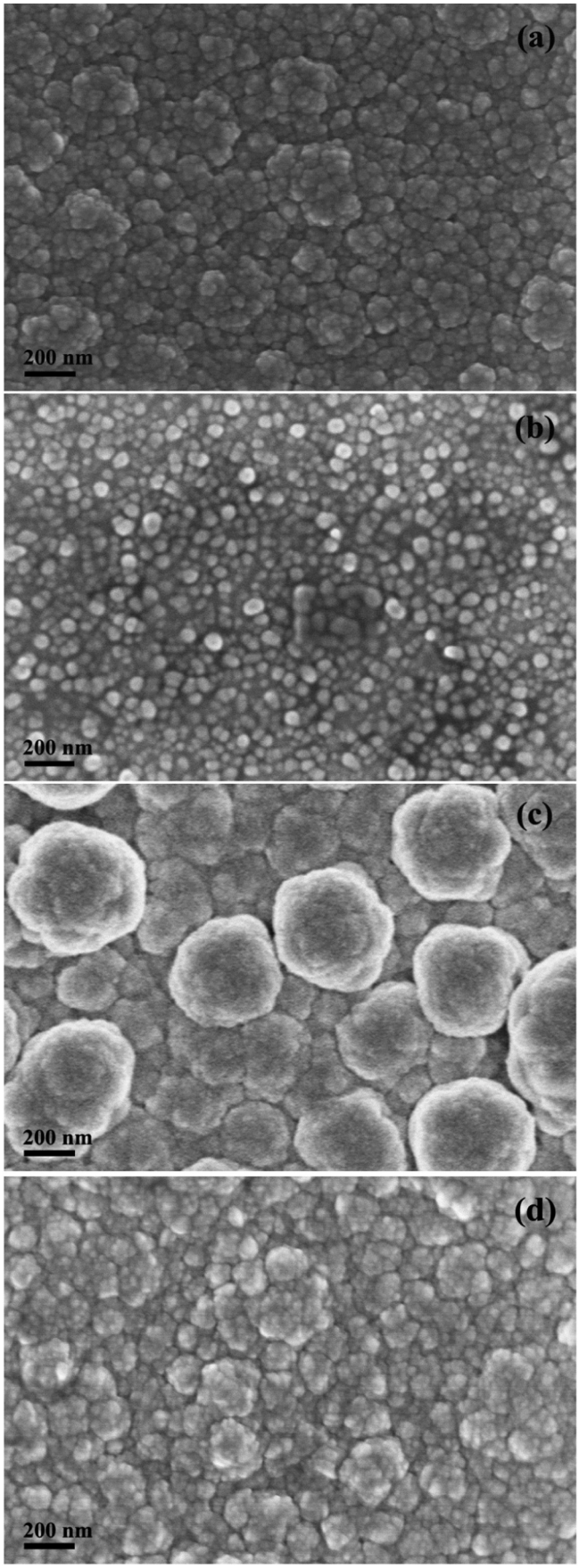

Fig. 1. The SEM surface morphological images of thin films deposited with the negative bias of 0 V (a), 50 V (b), 100 V (c) and 150 V (d).