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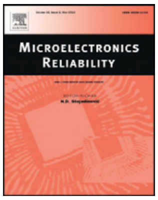

Evidence for causality between GaN RF HEMT degradation and the E_C-0.57 eV trap in GaN

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ABSTRACT

The degradation of industry-supplied GaN high electron mobility transistors (HEMTs) subjected to accelerated life testing (ALT) is directly related to increases in concentrations of two defects with trap energies of E_C-0.57 and E_C-0.75 eV. Pulsed I-V measurements and constant drain current deep level transient spectroscopy were employed to evaluate the quantitative impact of each trap. The trap concentration increases were only observed in devices that showed a 1 dB drop in output power and not the result of the ALT itself indicating that these traps and primarily the E_C-0.57 eV trap are responsible for the output power degradation. Increases from the E_C-0.57 eV level were responsible for 80% of the increased knee walkout while the E_C-0.75 eV contributed only 20%. These traps are located in the drain access region, likely in the GaN buffer, and cause increased knee walkout after the application of drain voltage.

Gallium nitride-based high electron mobility transistors (HEMTs) can demonstrate extraordinary RF performance due to their advantageous material properties and device design [1]; however, the high bias and power dissipation for which GaN HEMTs are intended can result in reduced long-term reliability and a need to understand and mitigate the factors that lead to reduced lifetime [2,3]. In RF circuits, variations in quiescent bias, current collapse, knee walkout, and a number of other dispersion phenomena can lead to loss of output power, increased non-linearity, and reduced gain among other things. Accelerated life testing (ALT) is used to predict device lifetime, but in many cases does not provide an obvious reason for the failure without significant post-mortem analysis using many other techniques to decipher the initial cases of degradation. Many of these degradation mechanisms are thought to result from activation, formation, or migration of electrically active defects behaving as traps, the presence of which can dictate device lifetime [3]. Constant drain current deep level transient spectroscopy (CI_D-DLTS) on fully-fabricated HEMTs is able to spatially resolve individual defects and quantify their concentration or change in concentration upon degradation, energy level, and capture cross section, which provides specific information on how specific traps evolve under ALT, DC bias stressing, etc. [4,5]. Prior work has revealed a dominant electron trap in GaN HEMTs located in the bandgap at E_C-0.57 eV, which has been detected by several methods [4,6]. This level was shown to increase in concentration with ALT testing and also track output power degradation that results from the ALT.

However, it is as yet not been made clear if HEMT degradation upon RF-ALT is due to this specific E_C-0.57 eV trap, since other defects and degradation mechanisms may also respond to the ALT; in other words there has not been a linkage of this trap to HEMT degradation that has been independent of the application of ALT. Here it is demonstrated unequivocally that the concentration of an E_C-0.57 eV level tracks the output power degradation and not just the application of RF biasing and/or high temperatures. Also, the concentration of a level at E_C-0.75 eV is shown to also track output power degradation, though with a much weaker dependence. These traps are responsible for virtual gating of the channel electrons, and the trap time constants derived from the CI_D-DLTS data match the drain lag time constants showing a clear, causal relation between these traps and the terminal characteristics of the HEMTs.

Four HEMTs from a single wafer from a single commercial vendor, grown by metal organic chemical vapor deposition (MOCVD), and characterized for the RF performance and trap spectra were subjected to accelerated life testing (ALT) to monitor the trap evolution with high temperature, high voltage stress. The device structures were relatively standard AlGaN/GaN structures with ~25% Al mole fraction, ~20 nm Al GaN barrier thickness, SiC substrates, SiN_x passivation and a source-connected field plate that was optimized for X-band at 40 V maximum V_{DS}. The HEMTs had gate peripheries of 400 μm and maximum output powers P_{out} of 2.5 W/mm, respectively, and were biased for Class AB operation with quiescent conditions of V_{DS} = 35 V and

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$I_{DS} = 205$ mA/mm for the RF measurements. Of the four HEMTs, three were subjected to ALT stressing at a 265 °C estimated channel temperature for HEMT2 and HEMT4 and 285 °C for HEMT3, operating at 10 GHz with an input power of 23 dBm, respectively, until a 1 dB drop in P_{out} was reached. The output power vs. time is shown in Fig. 1 where two samples (HEMT2 and HEMT3) degraded 1 dB in 1200 and 1550 h, respectively, while the third stressed device (HEMT4) lasted over 4000 h without significant degradation. The fact that HEMT3 failed before HEMT2 even though it was operated 20 °C cooler is due to statistical variation and not necessarily indicative of a non-Arrhenius degradation mechanism. Although not the focus of this paper, the threshold voltage V_T was not observed to shift significantly with ALT and traps under the gate were estimated with concentrations in the 10^9–10^{10} cm^{-2} range and were responsible for <5 mV transient shift in V_T.

To quantify the traps energies and concentrations in these HEMTs, the CI$_D$-DLTS technique was employed, where thermally-stimulated emission of carriers from traps is monitored in operational HEMTs. There are two modes, gate-control mode and drain-control mode, which allow detection of traps under the gate and in the access regions, respectively [4,7]. In both cases the drain current I_{DS} is kept constant by dynamic modulation of the gate or drain voltage, respectively, which allows a simple model to estimate the trap concentration and maintain a constant sensitivity to traps. This lateral spatial discrimination has previously been demonstrated, and the drain control CI$_D$-DLTS measurements have recently been corroborated by time-resolved scanning Kelvin probe microscopy (SKPM) [8]. The conventional double boxcar integration method is applied to the voltage transients that result from maintaining the constant I_{DS} where the trap emission rate can be determined as a function of sample temperature, which allows Arrhenius analysis to determine trap energies and thermal cross sections. The concentrations of the deep levels are obtained from the magnitude of the voltage transients. Drain controlled CI$_D$-DLTS, which is the focus of this work, is based upon dynamic control of the drain voltage V_{DS} in the triode regime to maintain a constant I_{DS} where the relationship between the trap concentration and drain access resistance change ($\Delta R_D = \Delta V_{DS}/I_{DS}$) is [4,7]

$$n_T = n_s^2 \left[n_s - \frac{L_{dep,\max}}{qW\mu \Delta R_D} \right]^{-1} \tag{1}$$

where $L_{dep,max}$ is the maximum lateral depletion region associated with the fill pulse (high V_{DS} in pinch-off), n_s is the two-dimensional electron gas (2DEG) concentration, W is the transistor width, μ is the 2DEG mobility, and n_T is the trap concentration. The depletion region $L_{dep,max}$ was estimated to be 0.15 μm by using a simple analytic equation developed to predict breakdown voltage in HEMTs that relates the applied drain-gate voltage [7,9], and initial SKPM measurements have corroborated the model predicted $L_{dep,max}$ [8]. Full details of the CI$_D$-DLTS/DLOS methods are available in Refs. [5,7].

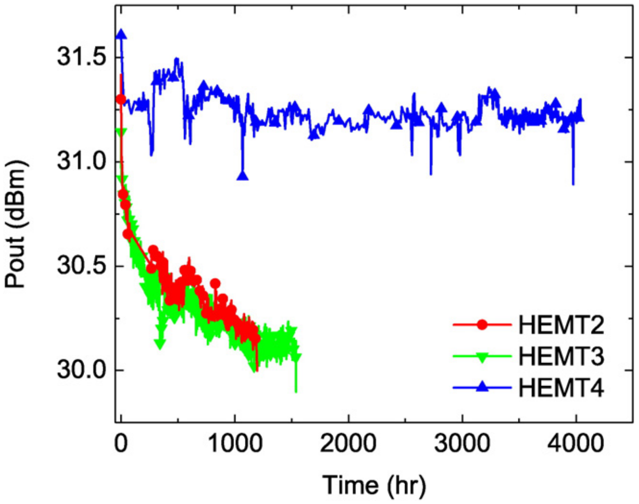

Fig. 1. Output power during accelerated life testing where HEMT2 and HEMT4 were subjected to Class AB operation with $V_{DS} = 35$ V and $I_{DS} = 205$ mA/mm DC conditions and 23 dBm input power at 10 GHz RF conditions is shown. The devices were stressed until a 1 dB drop in output power was observed or 4000 h in the case of HEMT4.

Fig. 2 shows the drain controlled CI$_D$-DLTS spectra for the four HEMTs where three regions are of interest. First, there is a dominant DLTS peak appearing at ~280 K in Fig. 2 of the post-stressed samples and is present for all samples. The inset of Fig. 2 shows the Arrhenius plot indicating that this trap is located 0.57 eV below the conduction band (E$_C$-0.57 eV) with a cross section of ~5×10^{-15} cm^2. This level is the dominant detected level in the two HEMTs that exhibited the 1 dB output power degradation and its influence on ΔR$_D$ is ~4-5× larger (0.43–0.5 Ω-mm) than on the unstressed HEMT1 (0.11 Ω-mm). This closely matches the results from multiple vendors reported in Ref. [9] and indicates the consistent role of the E$_C$-0.57 eV level in HEMT degradation. However, the key piece of data is that the non-degraded HEMT4 shows lowest ΔR$_D$ of the E$_C$-0.57 eV level (0.06 Ω-mm), even after the application of 4000 h of ALT stress among all the HEMTs studied here. This shows a clear relationship between 1 dB output power degradation and increased concentration of the E$_C$-0.57 eV level in HEMT2 and HEMT3 and not just application of stress.

The omnipresence of this level in MOCVD-grown HEMTs suggests this results from a common impurity or intrinsic defect formation, and the repeated correlation of the E$_C$-0.57 eV level signal with degradation and not just the stressing itself suggest that eliminating this level will improve reliability of these current state-of-the-art devices, but doing this requires knowledge of the physical source of this level. Recent comparison of HEMTs with AlInN and AlGaN where the E$_C$-0.57 eV level is commonly observed indicate this level is likely in the GaN buffer [10]. This level is also closely aligned in Arrhenius space with a GaN buffer trap commonly observed further suggesting the E$_C$-0.57 eV level is a GaN buffer trap [11–13]. Fig. 2b shows the HEMT and bulk GaN E$_C$-0.57 eV levels [14] and the close agreement between the levels. Work is currently underway to identify the trap activation mechanism, but these results indicate that further optimization of the GaN buffer is needed. An important feature to note is that the E$_C$-0.57 eV trap concentration increase is not correlated with increased gate leakage. Fig. 3 shows the gate leakage current during the ALT where only HEMT2 shows increased gate leakage, but both HEMT2 and HEMT3 showed increased E$_C$-0.57 eV. This indicates that although gate leakage is commonly observed to increase as the HEMT degrades, it itself is not necessarily an indicator of E$_C$-0.57 eV trap formation/activation especially when the gate leakage is relatively high at the beginning.

There are also two other features of the DLTS spectra in Fig. 2 worth noting. At the low temperatures, there is a broad shoulder in the CI$_D$-DLTS signal of every device except for the ALT stressed but non-degraded HEMT4 indicative of a possible broad band of shallow states near the conduction band edge. The indistinct nature of this peak prevents determination of a precise energy level, but traps in this temperature range would typically have an energy relative to the conduction of ~0.1–0.4 eV and at room temperature would have an approximate time constant of <~10^{-6} s. There is, however, no obvious correlation with the HEMT degradation. HEMT1 and HEMT2 have approximately the same ΔR$_D$ magnitude (~0.1 Ω-mm) and shape for this feature even though the former sample is unstressed and shows no power loss and the latter is stressed and degraded. Additionally, HEMT3 shows a 3× larger low temperature feature in Fig. 2 but was degraded 1 dB the same as HEMT2. Therefore, the presence and importance of this low temperature shoulder is not currently known, but the low magnitude in HEMT2 that showed significant degradation suggests that this level is of lesser importance.

The other feature of the DLTS is a high temperature peak in Fig. 2, which corresponds to an E$_C$-0.75 eV trap with a 1×10^{-14} cm^2 electron