Dual stacked gate dielectric source/oxide overlap Si/Ge FinFETs: proposal and analysis

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Abstract **—This paper proposes structures of two different FinFETs with conventional FinFET for different configuration of fin material and the orientation of the gate dielectrics over the source. One of the two new structures is a Silicon based trigate FinFET structure, where two gate dielectrics placed in stack and overlap to the source. The third structure is modified by replacing the Silicon fin with Germanium material with two stacked gate dielectrics overlap to the source. Since the best results being obtained from the third structure as less leakage current, and very high I_{ON}/I_{OFF} so, the further detailed analysis is done for the third structure by varying the various parameters length of source/oxide overlap, the dielectric thickness, and the fin widths.**

Keywords—dual dielectric; FinFET; Germanium; Silicon; source overlap.

I. INTRODUCTION

The reduction of the device dimensions of MOSFET such as scaling down of gate length, channel length, oxide thickness (t_{ox}) etc. causes the short channel effects (SCEs) [1]-[2], very high leakage current (I_{OFF}) and high value of subthreshold swing (SS). The scaling of t_{ox} causes the direct tunnel leakage current and the fluctuation of threshold voltage (V_{th}) and transconductance [3]. The Polysilicon gate depletion and the gate dopant penetration into the channel region also came into existence due to the reduction of gate oxide [4]. In order to limit the drawbacks of reduction of dimensions in MOSFET, also to assist the productive requirements according to the Moore's Law [5], there are various alternative novel devices have been looked out for. Based on the reducing the leakage current and having less SCEs, FinFET came into existence as propitious alternative to MOSFET. The FinFET structure is strong obstacle for the SCE due to its wrapping around nature of the gate over the channel. Since the channel is wrapped by the gate, the control of gate on the channel increases which decreases the leakage current (I_{OFF}) results in less SS, less SCEs such as less Drain induced barrier lowering (DIBL), and high on current (I_{ON}). There are various FinFET structures have been designed based on the functionality of the device which are based on the shape of the fin, and also the dimensions of the fin such as fin height and fin width including the obvious parameters as doping concentration of the channel, gate length, and gate dielectric thickness. The diverse FinFET structures which have been proposed as the Double Gate (DG) [6]-[8] FinFET, Tri-gate (TG) FinFET [8]-[9], Triangular shaped FinFET [10] etc. The Dual material gate FinFET suppressed the SCEs improving the carrier transport efficiency and the transconductance [15]. These effects can also be optimized by considering the gate length ratio and the work function difference [11]. A compact analytical scaling length model has been done for Tapered Tri Gate FinFET to physically understand the significance of the device and also the proposed model was compared with the existing rectangular FinFET [12]. The Trapezoidal triple gate FinFET [13], Gate-All around (GAA) Silicon (Si) FinFET [14], Omega shaped gate nanowire FinFET [15], and halo implant MuGFET [16] are also some of the FinFET structures which are already discussed to enhance the functionality of the device.

In this paper, we present two different FinFETs with conventional FinFET structure. The third new structure is modified by altering the material of the fin of the second structure with placing of dielectrics overlapping to gate source/oxide. The use of high k dielectric material increases the gate oxide capacitance resulting in less I_{OFF}. The use of Germanium (Ge) material, which is a low band gap material, increases the I_{ON} by a considerable amount.

This paper is organized as follows: section II describes the architecture of the devices with the simulation set up. The results of comparison of three different structures and the further analysis are shown and discussed in section III. Finally, section IV concludes the work.

II. DEVICE GEOMETRIES

The cross sections of three different structures are shown in the Fig. 1. The first structure is the conventional double gate FinFET named as Structure I, whereas the second structure is the modification of Structure I, named as Structure II, and the third one is the modification of second structure named as Structure III. In the Structure I, Silicon is used as a fin, hafnium oxide (HfO_2) (k=22), and Gate Polysilicon (Φ_m=4.25eV) are used as a gate dielectric material and gate material. The Structure II is a trigate FinFET structure, where SiO_2 (k=3.9) and HfO_2 are placed in stack and along with gate overlap to the source with Silicon (Si) as a fin material. Third structure (Structure III) is a slight modification of the Structure II, where Si is replaced by Ge material, where SiO_2 (k=3.9) and HfO_2 are placed in series and overlap to the source. In both the structures the length of each of source and drain is 5 nm. The overlap length of the Structure III is varied from 1 nm to the 7 nm. The concentration of the (n^+) source and (n^+)drain are 1×10^{20} cm^{-3} and p^+ channel is 1×10^{19} cm^{-3} and the other dimensions of the 3-D structures shown in Fig. 1

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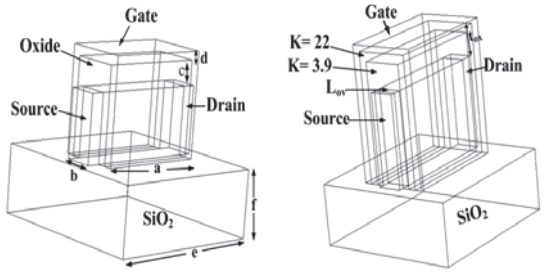
(a) and (b) are listed in the table I.



(a) (b)

Fig. 1. (a) 3 D view of the conventional and (b) gate source/oxide overlap FinFET structure (TCAD) (Structure II and Structure III)

TABLE I. DIMENSIONS OF FIG. 1

Parameter	Value (nm)
a	10-40
b	10
c	3
d	3
e	60
f	20

TABLE II. COMPARISON OF ELECTRICAL PARAMETERS OF STRUCTURES I, II, AND III OF FIG. 2

Structures	I_{ON} (A)	I_{OFF} (A)	I_{ON}/I_{OFF}	SS (mV/dec)
I	1.38×10^{-3}	1.74×10^{-10}	0.791×10^{7}	63
II	1.97×10^{-4}	1.02297×10^{-13}	1.925×10^{9}	79.7
III	1.41×10^{-4}	8.33×10^{-15}	0.167×10^{11}	83.3

The device structures are simulated by using the Synopsys TCAD [17]. To simulate the structures the Fermi Dirac Statistics has been used for proper distribution of carriers. However, the Bandgap Narrowing Model, Doping Dependent Mobility Model have also been used [17] to take into account the mobility of carriers since the higher doping concentrations are used which degrades the mobility of the carriers.

III. RESULTS AND DISCUSSIONS

A. *Comparison of transfer characteristics of Structure II and Structure III with the Structure I*

A comparative analysis between the Structure I, Structure II, and Structure III is described in this section. For this purpose, the transfer characteristics and the table containing the electrical parameters extracted from the three structures are shown in the Fig. 2 and table II. From the transfer characteristics and the table it is clarified that the I_{ON} and I_{OFF} is high for the Structure I. On the contrary, I_{ON} is slightly less and the value of Ioff is very less for the Structure II, and Structure III. For the Structure II, the value of I_{ON} is slightly less compared to Structure I, but the I_{OFF} is reduced by three orders of magnitude and as a result the Ion/Ioff ratio is very high, which is increased by two orders of magnitude compared to the Structure I. However, the Structure III shows a little less I_{ON} compared to Structure II, but the value of I_{OFF} is decreased more fascinatly. Since HfO_2 is a high k dielectric material it increases the capacitive effect resulting in high I_{ON} compared to the structure II. Moreover, the Structure I is a double gate FinFET structure, i.e. the control of gate on the channel decreases since the channel is surrounded by two sides only. In the structure II, a high k gate dielectric material (HfO_2) is used as a stack with the low k dielectric material (SiO_2) with Silicon as a fin. Due to the presence of high k gate dielectric beneath to the gate, it helps in reducing the gate fringing field emanating from the gate electrode. Moreover, the oxide overlap on source reduces the parasitic effects. That is why a very high value of Ion/Ioff i.e. 1.925×10^{9}, and less I_{OFF} (1.022×10^{-13}) is found which shows the reduction of Ioff up to three orders of magnitude and hence increase of Ion/Ioff up to two orders of magnitude compared to Structure I. The reduction of I_{OFF} is more when Si fin is replaced by Ge (Structure III). This can be explained with the help of the energy band diagram at gate voltage (Vgs) 0 V shown in Fig. 3.

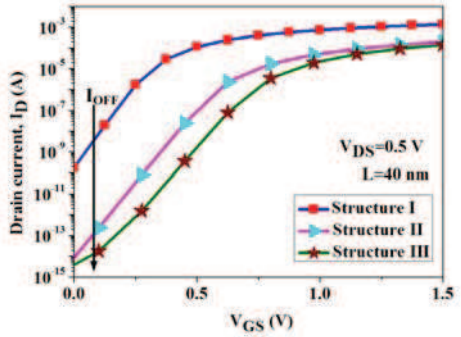


Fig. 2. Comparison of transfer characteristics of Structure I, Structure II, and Structure III

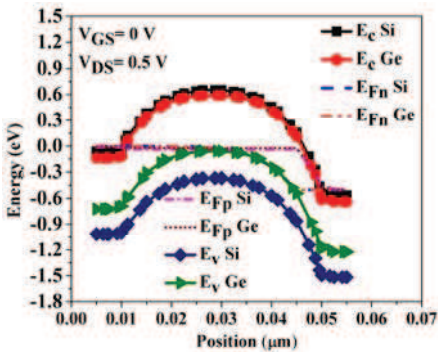


Fig. 3 Energy band diagram of Structure II and Structure III at V_{GS} 0 V

If we calculate the valence band position from the vacuum level in case of Germanium (Ge) i.e. (E_{vac}-E_v).