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Chip package interaction for LED packages

Sung-Uk Zhang

Samsung Electronics Co., Ltd., 1, Samsung-ro, Giheung-gu, Youngin-si, Geonggi-do 446-711, South Korea

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ABSTRACT

Solid-state lightings (SSL) rapidly penetrate the global illumination market because of the energy efficiency and the reliability. The energy efficiency can be easily evaluated but the reliability is not convenient to be estimated. Among several reliability issues, a LED chip level's reliability could be a difficult problem because chip failures related to electromigration phenomenon are hard to be detected in the early stages. In order to remove potential leakage LEDs in modules, additional screening method is necessary to be performed occasionally. In this study, chip package interaction (CPI) for LED packages was investigated in order to estimate stresses of the LED chip in the module level. This methodology would help LED manufacturers to perform a robust design of LED packages in terms of the LED chip reliability. The electromigration is related to metal diffusion, which belongs to a creep phenomenon. As the creep strain is a function of temperature, stress and time, quantifying stresses in the metal layers of the LED die can be useful information for LED manufacturers to make an engineering decision in the early stages of manufacturing.

1. Introduction

Solid-state lightings (SSL) rapidly penetrate the global illumination market because of the design flexibility, the energy efficiency, and the reliability. The design flexibility and the energy efficiency can be easily evaluated but the reliability is not convenient to be estimated. SSL is based on semiconductor and brings new manufacturing process and new materials, which introduces a series of new and unknown failure modes. Caers and Zhao have reported failure modes from device level to system level [1]. Among several failure modes, leakage failures are hard to be observed in device level or package level. Jeong et al. [2] reported the leakage from the mesa defects of P-N junction area in module level by using an accelerated life test. Fig. 1 shows the defect of a pin hole leaded to leakage failure of LED. The device level's reliability could not be considered with stress of system environment so that they developed a screening method to remove the potential leakage LED in the module. Pecht and Chang [3] have reviewed failure mechanisms and reliability issues in LEDs. Among them, semiconductor-related failure mechanisms are defect, die cracking, dopant diffusion, and electromigration. The electromigration leads to emergence of dislocations, point defects, leakage current and non-radiative recombination along the chip edges. They suggested proper thermal management in order to enhance the LED chip's reliability. However, sometimes the remedy is in conflict with the cost of LED packages and modules. Therefore, LED manufacturers need a robust design of the LED chips under limited conditions.

In this study, chip package interaction (CPI) for LED packages was investigated in order to estimate stresses of the LED die in the module level. The study of CPI has been conducted for integrated circuits packaging and interconnection technologies [4–12]. CMOS technology demands faster chips and lower power. In order to achieve the high performance, the application of porous low-k or ultralow-k dielectric materials brought the challenge of the structural integrity of CMOS chips. Similarly this methodology would help LED manufacturers to perform a robust design of LED packages in terms of the LED chip reliability. The electromigration is related to metal diffusion, which belongs to a creep phenomenon. As the creep strain is a function of temperature, stress and time, quantifying stresses in the metal layer of the LED die are useful for LED manufacturers in the early stages of manufacturing. This study only focused on evaluating stresses on the metal layers of LED chips. Computing creep strains using CPI would be further work. Moreover, this study assumed that stresses of metal layers are related to the electromigration. The verification will be further work.

2. Methodology

This section is divided into three subsections. The first subsection introduces a structure of an LED chip. This structure includes four composite metal layers. For a simplification of these metals, a homogenization technique is introduced in the second subsection. Finally, the finite

E-mail address: sunguk.zhang@samsung.com.

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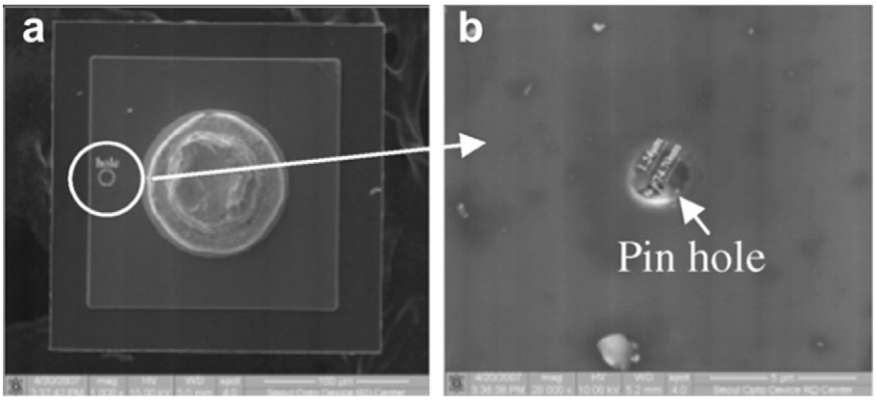

Fig. 1. LED Leakage failure occurred by defect of pin hole [2].

element method using a sub-modeling technique is described for CPI in the LED package.

2.1. LED chip structure

Krames et al. [13] have reported status and future of high-power LEDs. The LED designs are divided into AlGaInP (red to yellow) and InGaN LEDs (blue to green) according to external quantum efficiency at peak wavelength. The AlGaInP LED designs are thin epilayers on GaAs absorbing substrate (AS), thick AS, thick AS design but including distributed Bragg reflector (DBR) above substrate, thick window layer on transparent substrate (TS), shaped TS, and thick window layer on reflective substrate (RS). In the other hand, common chip designs for sapphire-based InGaN-GaN LEDs include "epi-up" conventional chip (CC) with semi-transparent top p contact, flip-chip (FC) with reflective p contact, vertical-injection thin-film (VTF) bonded to reflective metal on host substrate, and thin-film flip-chip (TFFC). Among above LED chip designs, this paper focuses on the flip-chip (FC) with reflective p contact. Simple fabrication processes of the FC are shown in Fig. 2. Four sequential processes are introduced. Firstly, LED mesas and n-contact are defined by using photolithography and etching process. Secondly, p-type metal contacts and n-type metal contacts are formed with composite metal layers such as Cr/Al/Cr/Au [14,15]. Thirdly, silicon oxide layers are deposited for passivation and isolation of the p- and n-electrodes. Finally, bond metal layers are deposited above two electrodes, which are also composite metal layers like Ti/Al/Ti/Au [14,15].

2.2. Numerical homogenization technique for composite metals

Composite metals such as above mentioned metal contact layers and bond metal layers are applied as multilayer Ohmic contact schemes in order to maintain good Ohmic contact and thermal stability and luminous intensity [14,15]. Modeling the multilayer contacts is computationally expensive so that equivalent material properties of the multilayer Ohmic contacts were computed and used for CPI. The equivalent orthotropic properties for the composite metals were calculated using seven load cases that are three tensile loads, three pure shear loads and one thermal load for a representative volume element model (RVE) [7,8]. Fig. 3. shows four examples for RVE of which the size is one cubic millimeter. The size of RVE does not vary with the

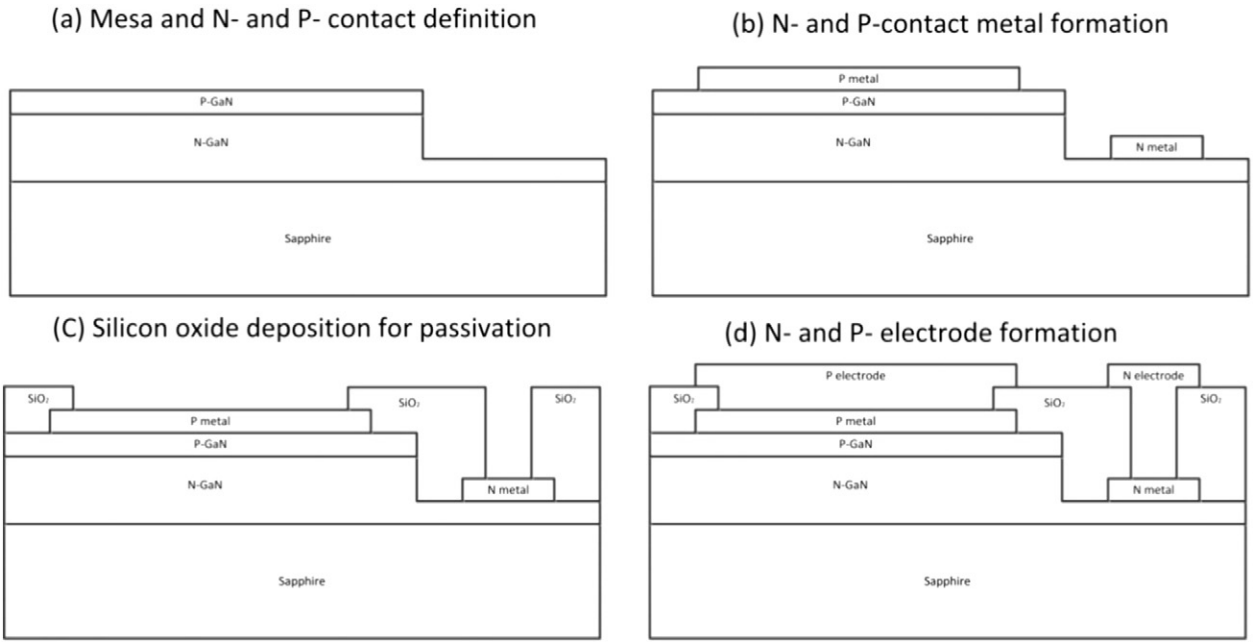

Fig. 2. Fabrication processes for a FC with reflective p contact.