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Investigation into sand mura effects of a-IGZO TFT LCDs

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ABSTRACT

The reliability of liquid crystal display (LCD) panels based on amorphous indium-gallium-zinc oxide thin-film transistors (a-IGZO TFTs) is investigated. It is revealed that the a-IGZO TFT LCDs also have sand mura issue at high operation temperature. Analysis shows that the sand mura is caused by the positive V_{th} shift of the a-IGZO TFTs. To suppress the V_{th} shift, fabrication process of the a-IGZO TFTs is optimized with a-IGZO channel layer annealed at 300 °C and etch-stop layer deposited at 250 °C. The process optimization lessens the absorbed and non-bonded oxygen atoms in the a-IGZO channel layer and desorbed water molecules on the back channel surface. The results show that the V_{th} shift is significantly alleviated and the sand mura is thus effectively minimized with the optimized process.

1. Introduction

Recently, amorphous indium-gallium-zinc oxide thin-film transistor (a-IGZO TFT) have attracted much attention due to their high mobility, excellent uniformity over large area, good bending performance, and high transparency to the visible light [1–3]. They have been considered to be the most promising devices for application in the next generation displays, such as active-matrix organic light-emitting diodes (AMOLED) and flexible displays. With the superior device characteristics a-IGZO TFTs are also now being used to manufacture high definition and high performance active-matrix LCDs which cannot be implemented by the currently prevalent a-Si TFT technology [4]. It has been reported that V_{th} shift of the a-IGZO TFTs under electrical stress is also an issue which would become a major concern of the a-IGZO TFT based LCDs and OLEDs [3,5]. The dependences of the V_{th} stability of a-IGZO TFTs have been much investigated on the fabrication processes of gate insulator (GI), a-IGZO active layer, passivation layer and so on [6–11]. However, the impacts of the V_{th} stability on the reliability of the a-IGZO TFT based display products have not been addressed yet so far.

In this work, sand mura effects of a-IGZO TFT LCDs are investigated. To manifest the mechanism behind the a-IGZO LCD sand mura issue, a series of tests such as the macroscopic picture, the microscopy picture, adjusting gate driving voltage and the thermal gate bias stress of a-IGZO TFTs are carried out. An optimized a-IGZO TFT fabrication process is proposed to minimize the sand mura effect, and the availability of the proposed process for improving the reliability of the LCD module based on a-IGZO TFTs are also verified.

2. Experimental details

Fig. 1 shows the cross-sectional schematic diagram of the a-IGZO TFTs fabricated in this work. Eagle XG glass was used as the substrate. Conventional etch-stop layer (ESL) process was used to fabricate the a-IGZO TFTs [2]. First, a 200 nm Mo layer was deposited by DC magnetron sputtering and patterned to form the gate electrode (GE) by wet etching. A single 250 nm SiO_x layer was then deposited as gate insulator (GI) by plasma enhanced chemical vapor deposition (PECVD) at 290 °C. Afterwards, a 50 nm a-IGZO active layer was deposited by using DC magnetron sputtering from the target of In_2O_3:Ga_2O_3:ZnO = 1:1:1 mol% in Ar and O_2 mixture gas at the room temperature. The active island was then patterned by wet etching, followed by an annealing treatment at 300 °C. A 100 nm SiO_x layer was then deposited as ESL at 150 °C or 250 °C by PECVD, and source and drain contact holes were then formed by reactive ion etching (RIE). The ESL SiO_x layer on the a-IGZO protects the channel layer from etchant damage during the source/drain wet etching. Following that, a 200 nm Mo layer was deposited by DC magnetron sputtering and patterned to form source and drain electrodes by wet etching. Then, a 40 nm ITO was deposited by using DC magnetron sputtering at room temperature and patterned

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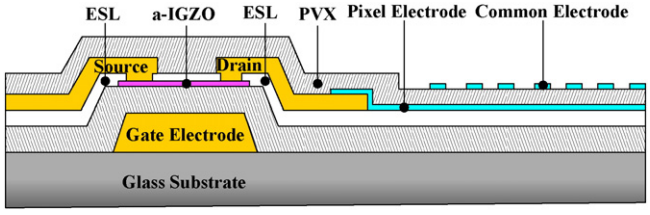

Fig. 1. Cross-sectional schematic diagram of the a-IGZO TFTs fabricated in this work.

by wet etching to form transparent pixel electrodes. Next, a 300 nm SiO_x passivation layer was deposited by PECVD at 290 °C. RIE was used to form PAD contact holes. Finally, the second transparent conductor layer of 80 nm ITO was deposited by DC magnetron sputtering and patterned to form common electrode by wet etching. The post-annealing was carried out at 300 °C in air atmosphere for 1 h.

Note that the advanced super dimension switch (ADS) technology was utilized to fabricate the LCD modules to improve the view angle of LCD [12]. The ADS adopts the transparent ITO as the common electrodes, which used to be metal in conventional process, leading to the increment in the aperture ratio and transmittance.

3. Results and discussions

Fig. 2 shows the transfer characteristics of the fabricated a-IGZO TFTs with reference process at different V_{DS}. The saturation mobility (μ_{sat}) and threshold voltage V_{th} are derived from the linear fitting of the $I_{DS}^{1/2}$–V_{GS} plot in saturation region according to the following equation:

$$I_{DS} = (\mu_{sat} C_{ox} W/2L)(V_{GS}-V_{th})^2, \quad (1)$$

where I_{DS} is the drain current in saturation region and C_{ox} is the gate capacitance per unit area. The sub-threshold swing (SS) is the minimum value taken from

$$SS = (\partial \log I_{DS}/\partial V_{GS})^{-1}, \quad (2)$$

where I_{DS} is the drain current in the sub-threshold regime.

As shown in Fig. 2, the a-IGZO TFT for ADS-LCD shows good performance with a mobility of 11.7 $cm^2/V \cdot s$, V_{th} of 1.4 V, and SS of 0.39 V/dec at V_{DS} of 10 V.

Four-inch ADS-LCD modules based on two sets of a-IGZO TFTs processes are assembled to investigate the reliability. In the reference process, the a-IGZO TFT is without any annealing process for IGZO film and

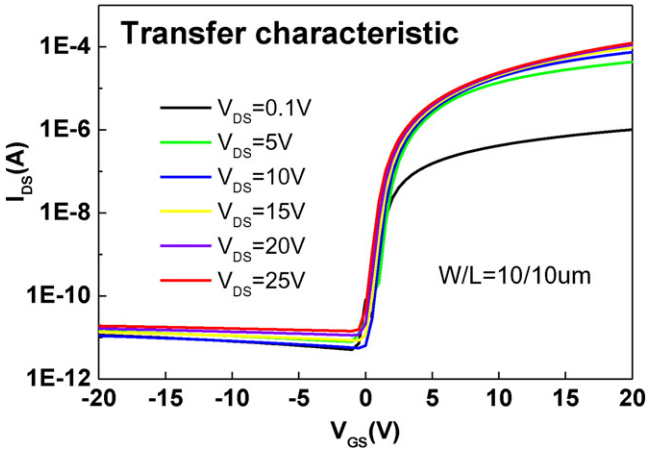

Fig. 2. Transfer characteristic of a-IGZO TFTs for ADS-LCD with the reference at different value of VDS.

with a low temperature of 150 °C for ESL deposition. In optimized TFT process, a 300 °C annealing process is conducted for a-IGZO film before ESL deposition. Moreover, a high temperature of 250 °C for ESL deposition is adopted. It is well known that ADS-LCD operates in normally black mode. In this paper, pixels show dark state when V_{GS} is −12 V (off state of TFT) and show white state when V_{GS} = 8 V(on-state of TFTs).

Fig. 3 (a) shows the picture of a normal display module under white state with good display quality. Fig. 3 (c) is the corresponding microscopic image of its RGB sub-pixels under on state. The RGB pixel is switched on uniformally. For comparison purpose, in Fig. 3(b), an abnormal display module with sand mura is shown. It contains a lot of abnormal black dots under white state. The sand mura is the main issue of ADS-LCD reliability test at 80 °C operation [3]. Compared with the normal display in Fig. 3(a, c), most sub-pixels of the abnormal display in sand mura area show dark state at VGS = 8 V in Fig. 3(d), indicating that the a-IGZO TFTs are under off state. It is thus inferred that the Vth of a-IGZO TFTs in sand mura area has a large positive shift during the reliability test.

For further investigating the origin of sand mura, the gate driving voltage (V_{GS}) of a-IGZO TFT backplane under on state in sand mura area are adjusted from 8 V to 12 V and 16 V, respectively. Most sub-pixels turned from dark state to white state when gate driving voltage increased to 12 V as shown in Fig. 4(b). Furthermore, with the gate driving voltage further increases to 16 V, they completely become normal in Fig. 4(c), indicating that all the a-IGZO TFTs in sand mura area are under on-state. That is, the sand mura occurred in ADS-LCD reliability test is very likely caused by the positive V_{th} shift of a-IGZO TFTs.

It has been reported that improving GI process, optimizing a-IGZO process, using a high quality ESL or conducting post annealing can effectively improve the V_{th} stability of AOS TFTs [13–17]. In this work, an optimized process for a-IGZO TFTs fabrication is proposed, where a 300 °C annealing process before ESL deposition and a high temperature deposition for ESL at 250 °C are performed to improve the V_{th} stability of a-IGZO TFTs.

To further confirm the reason of sand mura caused by positive V_{th} shift of a-IGZO TFTs in reliability test, positive gate bias temperature stress (PBTS) of a-IGZO TFTs is also carried out. The gate, drain and source voltages were fixed at 30 V, 0 V and 0 V during the electrical stress period. Fig. 5 shows the variations of the transfer characteristics of the fabricated a-IGZO TFTs with different processes under the PBTS for 7200 s at 80 °C. It is observed that the device with the reference process has a significantly positive Vth shift up to 15.2 V without noticeable SS change in Fig. 5(a). While for the device with the optimized processes, it exhibits a small Vth shift of 0.76 V as shown in Fig. 5(b).

It is well known that the parallel V_{th} shift of a-IGZO TFTs under electrical stress, thermal electrical stress or illumination is mainly due to the charge trapping in the channel layer or at the interface of passivation/channel layer or GI/channel layer [8–11]. During a-IGZO deposition, the a-IGZO film for channel layer adsorbed some extra oxygen atoms from oxygen plasma. These extra oxygen atoms were non-bonded with metal ions. It is reported that the adsorbed oxygen atoms captured electrons from the conduction band and formed negative traps such as O^{2-} or O^- ions, resulting in positive V_{th} shift of TFT under gate bias stress [18]. Therefore, for the device with reference fabrication process, the electrons in the channel would be captured by adsorbed oxygen atoms then formed the negative potential V leading to the V_{th} shift.

It is seen that the film density of SiO_x for ESL at 250 °C is significantly better than that of 150 °C, with less pinhole defects shown in Fig. 6. In the other words, the SiOx film deposited at 250 °C for ESL layer is better than that deposited at 150 °C to prevent water molecules penetration into the a-IGZO back channel surface. It is also reported that water molecules on surface of the back channel desorbed under the positive gate bias stress resulting in an increase of positive V_{th} shift [18,19], due to