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Realization Of Ternary Reversible Circuits Using Improved Gate Library

P. Mercy Nesa Rani[a,*], Abhoy Kole[b], Kamalika Datta[a], Alok Chakrabarty[a]

[a]*Department of computer Science& Engineering, National Institute of Technology, Shillong 793003, India*
[b]*Department of Computer Application, B. P. Poddar Institute of Management & Technology, Kolkata 700052, India*

Abstract

Ternary logic has some distinct advantage over binary logic. In this paper we propose a synthesis approach for ternary reversible circuits using ternary reversible gates. Our method takes a boolean function as input. The input is provided as .pla file. The .pla file is first converted into ternary logic function, which can be represented as permutation. The gate library used for synthesis is Ternary Not, Ternary Toffoli and Ternary Toffoli$^+$ (N_T,T_T,$T_T{}^+$). The proposed constructive method, generates 3-cycles from the permutation, and then each 3-cycle is mapped to (N_T,T_T,$T_T{}^+$) gate library. Experimental results show that the method generates lesser number of gates for some circuits compared to previously reported works.

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1. Introduction

Multi-valued logic (MVL) has got several advantages over the binary logic in quantum computation *viz.,* better security for quantum cryptography and more power for quantum information processing. Among the MVL realization of quantum circuits, three-valued logic (ternary logic) plays an important role and is termed as qutrit (quantum ternary digit). The amount of information that can be stored per bit for ternary logic is more as compared to the binary logic. It is expected that qutrit-based quantum information processing will be more powerful than qubit (two-valued) implementation.[13] As a result, many researchers have proposed ternary quantum logic synthesis approaches.[8 5 12] There are two approaches for ternary reversible circuit synthesis which includes group theory based approach and Genetic Algorithm (GA) based approach.There exists some group theoretic approaches in literature for synthesis of ternary reversible circuits[18 15 17] which synthesizes the circuits using different gate libraries. Li et al.[10] proposed the synthesis of ternary non-reversible circuits using the ternary Swap, Not and Toffoli (SNT) gates. They converted the non-reversible ternary logic circuits into ternary reversible logic circuits and obtained 3-cycles from the given boolean function which are decomposed into the product of neighbouring 3-cycles. Then the neighbouring 3-cycles

* P.Mercy Nesa Rani, Tel.: 91-0364-2501294 Fax.: 91-0364-2501113
E-mail address: mercyrani@nitm.ac.in

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are synthesized using SNT gate library which increases the gate count to synthesize the circuits but reduces the number of ancilla input and garbage output bits. GA based synthesis of ternary reversible circuits have been reported in[2 11 9] that has a large search space for solving problems in reversible circuits and the successful selection of fitness function is very important to achieve the convergence for search solution.
In this paper, we develop a group theory based ternary reversible synthesis method, which require the ternary Toffoli, ternary toffoli$^+$ and ternary Not gates to synthesize the ternary reversible circuits. The use of (N_T,T_T,$T_T{}^+$) gate library helps in the reduction of gate count as compared to existing work[10]. The rest of the paper is organized as follows: Section II presents the basic concepts of ternary reversible gates. The proposed approach with an example to realize the ternary reversible circuits are given in section III. Section IV summarizes the experimental results for some benchmarks followed by conclusion in section V.

2. Basic Concepts and Ternary Reversible Gates

In this section we discuss about ternary reversible gates and circuits. In a general form a ternary reversible gate can be defined in the following way:

Definition 1. *A ternary reversible gate with n-inputs represent a bijection of:* $T^n \rightarrow T^n$ *where T denote the set of ternary logic values* $\{0, 1, 2\}$.

In synthesizing the circuits, gates are added to the circuit in order to realize the desired functionality. Like binary reversible circuit, a ternary reversible circuit is defined as:

Definition 2. *A ternary reversible circuit represents a cascade of ternary reversible gates, i.e.,*

$$C = T_1 T_2 \dots T_{\mathfrak{R}} = \bigcap_{i=1}^{\mathfrak{R}} T_i$$

without any feedback or fanout.

The outputs of a ternary reversible function is a *permutation* of its inputs.

Definition 3. *A permutation on* $M = \{d_1, d_2, \dots, d_n\}$ *is a bijection of M onto itself,* $M \rightarrow M$.

The set of all permutations on inputs, forms a group under composition of *mapping*, called symmetric group S_k[3]. A permutation group is simply a subgroup of a symmetric group. A mapping $S : M \rightarrow M$ can be written as a product of disjoint cycles.

Example 1. *For the inputs* $\{d_1, d_2, d_3, d_4, d_5, d_6, d_7, d_8, d_9\}$ *one possible mapping is*

$$mapping = \begin{pmatrix} d_1 & d_2 & d_3 & d_4 & d_5 & d_6 & d_7 & d_8 & d_9 \\ d_1 & d_4 & d_7 & d_2 & d_5 & d_8 & d_3 & d_6 & d_9 \end{pmatrix}$$

which can also be written as a composition *of* (d_2, d_4), (d_3, d_7) *and* (d_6, d_8).

Definition 4. *For a given group of symbols* $d_1, d_2, \dots, d_n \in S_n$ *a mapping* $d_{i1} \rightarrow d_{i2} \cdots \rightarrow d_{ik} \rightarrow d_{i1}$, *where* $k \leq n$ *and* $1 \leq i1, i2, \dots, ik \leq n$ *is called a k-cycle denoted as* $(d_{i1}, d_{i2}, \dots, d_{ik})$.

In realizing the reversible circuits, Toffoli gate is used extensively in binary domain. In ternary domain the funtionality of the gate is extended and the gate is termed as Ternary Toffoli gate.

Definition 5. *A ternary Toffoli gate* $T(\{B_2, B_3\}; B_1)$ *is defined such that if the state of control qutrits* $B_2, B_3 \in \{1, 2\}$ *and* $B_2 = B_3$, *then the state of target qutrit* B_1 *is realized as* $P_1 = B_1 \oplus_3 1$, *where* $\oplus_3$ *stands for addition modulo 3; otherwise,* $P_1 = B_1$, *whereas* $P_i = B_i$, *for* $i \neq 1$.

In other words, (B_1, B_2, B_3) maps to $(B_1 \oplus 1, B_2, B_3)$ using modulo 3 addition when $B_2, B_3 \in \{1, 2\}$ and $B_2 = B_3$. Fig. 1 shows a Ternary Toffoli gate and its corresponding truth table is presented in Table 1 where $X \in \{0, 1, 2\}$.

The operation of a ternary reversible gate can be realized using a cascade of elementary multi-valued M-S gates that can be implemented using ion-trap technology[14].