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A holistic review of mismatch loss: From manufacturing decision making to losses in fielded arrays

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ABSTRACT

Mismatch loss relating to difference in as-manufactured cell performance is known to be nearly non-existent in a modern, undamaged, photovoltaic module. At a system level, potential contributors to this loss can include manufacturing variance, uncertainties in cell and module performance measurements and variation in operating conditions in the field. While some of these aspects have been individually studied, often using idealised performance models, there lacks a holistic treatment that assesses all the contributing effects in the same context. This is particularly important given the potential for trade-off among some of the underlying loss mechanisms in the way cells and modules are grouped and installed. This study shows, using a hybridised approach of published studies, manufacturing data, field performance data, and performance and variance modeling, that mismatch loss remains a potentially important performance loss mechanism in many photovoltaic installation. The decisions made in manufacturing pertaining to mismatch loss are found to often have only a small impact, despite potentially adding cost and complexity to the process. Conversely, field installation issues are shown to be of dominant importance in the final mismatch loss estimate. Understanding the individual contributing mechanisms, all together, will allow for the development of a realistic and least cost approach to mitigating the loss right from the decisions made in manufacturing through to how the modules are installed in the field.

1. Introduction

A single photovoltaic cell has a current / voltage characteristic such that it will only produce its maximum power (P_{mp}) at a single current / voltage pairing, known respectively as the maximum power point current (I_{mp}) and maximum power point voltage (V_{mp}). To generate a significant amount of power single cells must be interconnected to form modules, and those modules interconnected to form arrays. Photovoltaic (PV) devices all differ slightly in their current / voltage characteristics due to manufacturing variance and also variance in the operating conditions they experience. So in a fielded array, the individual cells will all operate at some deviation from their individual maximum power capability. This will cause a small loss in power and the sum of these losses across the entire array is known as the "mismatch loss". Mismatch losses due to manufacturing variance is typically managed by sorting products into "categories" or "bins". The sorting will have an impact on the variance of the final modules, which will in turn impact on the way they are deployed in the field.

Many studies already deal with individual aspects of mismatch loss and these are reviewed in Section 2. It is the unique aim of this study to compare and contrast the potential sources of mismatch loss in a single study, most particularly to include unavoidable real-world effects associated with variance in manufacturing and variance in the conditions experienced in the field. Several new and novel elements are introduced, including -

- A method to simulate a distribution of modules from a distribution of cells that accounts for real-world manufacturing variance effects,
- Simplified methods for calculating the mismatch loss from cells and modules based on the properties of the interconnected devices
- The in-situ calculation of likely mismatch loss in a fielded array

It should be noted that the focus of this paper is to examine sources of mismatch that occur in fault-free cells and modules, subjected to the expected manufacturing variance conditions. It is *not* intended to deal with situations involving faulty or damaged cells and modules, partial shading, or effects associated with aging and degradation of cells and modules over the life of the installed system [1]. These are all important effects, and many of the techniques introduced here are applicable to those situations. But the occurrence probability of all these events is

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generally unrelated to the manufacturing decisions that are examined in this study. The mitigation strategy will generally be different for these types of faults, and they should be examined as part of a separate study.

2. Overview: manufacturing issues that impact mismatch loss

This section reviews the theory of mismatch loss as related to series and parallel interconnection. This is then used as a basis to understand the mechanisms which impact mismatch loss from a perspective of the decisions made when manufacturing modules.

2.1. Theoretical mismatch loss for series and parallel interconnection

For the series interconnection of either cells or modules (referred to generically as “devices”), mismatch loss is proportional to the variance of the maximum power point current [2,3], as represented by Eq. (1),

$$Series\ \ Loss\,(\%) \propto \sigma_{I_{mp}}^{2} \tag{1}$$

where $\sigma_{I_{mp}}$ is the standard deviation in I_{mp} of the devices being interconnected, as a proportion of their average. This is known as the “relative standard deviation”, and all of the standard deviation quantities in this study are relative standard deviation values unless otherwise specified. A typical value for this standard deviation, from the 2012 production data used in this study is in the range of 0.5–0.6%, resulting in a loss in the range of 0.02–0.04%. The constant of proportionality in Eq. (1) can be derived through a variety of means, and this is discussed in Appendix B. Eq. (1) is applicable only where all of the devices being interconnected are operating in forward bias, or in other words, the I_{mp} value of every device is less than the average short circuit current (I_{sc}) of all the cells being interconnected. When this condition holds, the maximum power point current (I_{mp}) of a series interconnection of cells will operate very close to the average I_{mp} of all the cells [3], not at the lowest I_{mp}. The latter assumption is a common misconception originating from when cell variance was generally much higher. In the case of cell faults or shading [4–9] the difference in performance between cells is often too large, and Eq. (1) no longer applies. In this situation the classic notion of a series connection of cells being limited by the cell with the lowest I_{mp} is once again true, and other methods are required to calculate mismatch loss.

A similar relationship also applies to mismatch loss from parallel interconnection [2], shown in a simplified form in Eq. (2).

$$Parallel\ \ Loss\,(\%) \propto \sigma_{V_{mp}}^{2} \tag{2}$$

where $\sigma_{V_{mp}}$ is the standard deviation in V_{mp} of the devices being interconnected, again as a proportion of their average. The equation is applicable for a much wider range of values for the standard deviation in V_{mp}, as there is not the same risk of a reverse bias fault undermining the relationship as there is for the series interconnection. The applicability of the relationship and the constant of proportionality are discussed in Appendix B.

2.2. Module level mismatch loss (cell-to-cell variance)

When cells are interconnected to form a module, there is mismatch loss due to variance in the cell's performance and this is referred to here as “module level” mismatch loss. In most modules, cells are interconnected in series and so Eq. (1) primarily applies. Historically, this is a well studied and documented effect [2,10–13] but in a modern photovoltaic module the effects is so small it is virtually un-measurable [14,3], due to low variance in the cell performance in mass production.

Nonetheless, when photovoltaic cells are manufactured, they are regularly sorted into bins based on the current or power of the cell. The primary aim of this sorting is to further reduce an already low cell-to-cell variance. Every time a bin fills with enough cells to make a module - typically 60 or 72 - these cells are grouped together into a “cell packet”. The cells in this cell packet will later be interconnected to form a module. The average electrical performance properties of the cells in the cell packet will primarily determine the electrical performance properties of the module made from those cells. This is not perfectly deterministic because some variance is introduced during the module-manufacturing process, due to variance in the tabbing and string process, bill of materials and other effects. This is referred to as Cell-to-Module Variance (CTMV), and it is discussed further in Section 2.5.

2.3. Array level mismatch loss (module-to-module variance)

When modules are interconnected in a fielded array, variance in the module's performance results in “array level” mismatch loss. In a fielded array, modules are typically interconnected firstly in series “strings” and for that Eq. (1) will apply. These strings are then often connected in parallel, which introduces the additional loss as expressed by Eq. (2) due to the variance in the V_{mp} of all the strings connected in parallel. Appendix B provides information on choosing the proportionality constant in the loss equations. To minimise these losses, modules can also be binned by their I_{mp} and P_{mp}. Studies on array-level mismatch loss [15,6] typically look at theoretical models of how to bin modules and install them in the field to minimise loss. Webber and Riley [?] attempt to quantify the significance of mismatch loss in the context of a large solar installation selling energy at a given agreed price. They note that binning modules to reduce array level mismatch loss is not a zero cost exercise and should only be done with an understanding of the value it delivers.

2.4. Trade-off between module and array level variance

Decisions about cell sorting are a trade-off between cell-to-cell variance within a module, and module-to-module variance within the array. If the cells are sorted into more bins, each with a narrower range of performance properties, the variance within each bin and therefore each module will be very small. But consequentially, the variance between the average cell packet properties, and therefore the final module properties, will be greater. Module binning can then be done to control the module variance that is created by cell binning. Conversely, if there are fewer cell bins or no cell binning whatsoever, the variance within each cell bin is much larger, but the average cell packet properties and therefore the final module properties will have a much lower variance. These two variance components will sum to give the total variance as expected from fundamental statistical theory [?], as given by Eq. (3).

$$\sigma_{pop}^{2} = \sigma_{wcp}^{2} + \sigma_{cpAv}^{2} \tag{3}$$

where σ_{pop}^{2} is the population variance in production, σ_{wcp}^{2} is the (pooled) variance within the cell packet and σ_{cpAv}^{2} is the variance of the cell packet average. Given that the term on the left hand side, σ_{pop}^{2}, will be a constant for a given production situation, the cell binning is really just a decision about the relative size of the terms on the right side of Eq. (3). This relationship of Eq. (3) will hold true for any given cell performance parameter, but typically I_{mp} or P_{mp} is used for bin sorting. This trade-off is also discussed in the literature. Pavan et al. [16] note that cell sorting into tighter ranges will reduce variance within a module but result in modules with a wider range of performance which must be dealt with at the installation level. Iannone et. al. [17] also discuss this trade-off, noting the higher costs involved in field installation when managing modules with different current and voltage ratings. There is no detailed quantitative discussion of this trade-off.

2.5. Cell to module variance (CTMV)

When cells are interconnected and then encapsulated behind glass to form modules, it is well known that there is some change in the