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Impact of contact integrity during thermal stress testing on degradation analysis of copper-plated silicon solar cells

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ABSTRACT

In this study, silicon solar cells with copper-plated front side metallisation were exposed to long-term reliability thermal stress conditions and the material integrity of the plated contacts after stress testing was investigated using imaging and electrical measurements. Significant voltage 'bend-back' was observed in Suns-V_{OC} measurements at high illumination intensities (> 1 Sun) following thermal stress testing at 200 °C for 500 h of laser-ablated cells with a nickel/copper/silver plated front metal grid. Using a combination of focussed ion beam milling, high resolution imaging and energy dispersive X-ray spectroscopy, it was shown that large voids can form between the silver capping layer and the main copper stack during thermal annealing. However, even more revealing was the detection of a new metal layer comprising largely of diffused copper overlying the silver capping. The cause of the Schottky 'bend-back' behaviour was theorised to be due to increased contact resistance arising from the voids which are presumed to form as a result of grain boundary diffusion of copper through the silver capping layer. Errors of 5–10% in the determination of *pFF* from Suns-V_{OC} occur as a result, with the scale of the error dependent on the capping method and sintering conditions. Collapsing the voids was subsequently shown to remove the Schottky behaviour and improve reliability of the fitted diode parameters extracted from Suns-V_{OC} measurements.

1. Introduction

Front contact metallisation, which is predominantly achieved by silver (Ag) screen-printing, remains one of the most costly and critical steps in solar cell production [1]. Copper (Cu) plating is frequently presented as the obvious candidate to replace screen-printing, offering lower cost and higher performance capabilities, with plating-based technologies expected to hold increasing market share (~10%) over the next 10 years [2,3]. Despite this, widespread adoption of plating in industrial cell manufacturing is slow due to several issues, namely metal contact adhesion to silicon (Si) and long-term reliability concerns related to Cu penetration into the underlying Si wafer [4]. Copper is highly mobile and can diffuse readily in silicon where, in sufficient concentrations, it can lead to significant degradation in a cell's electrical performance due to the formation of recombination centres typically including Cu precipitates [5–7]. To mitigate this issue, an intervening metal layer is often employed as a diffusion barrier, with nickel (Ni) most commonly used in plated solar cells [8,9]. However, variability in barrier quality can reduce its effectiveness [10–12] and thus some form of reliability testing is required to assess the stability of plated barrier layers on silicon solar cells.

In order to study the reliability of plated solar cells, an accelerated aging test was reported by Bartsch et al., whereby plated cells are exposed to elevated temperatures for extended periods to simulate long term operation, with a reduction in pseudo fill factor (*pFF*) being used as an indicator of copper-related degradation [13]. By monitoring *pFF*, the effects of series resistance in the cell are eliminated, thereby providing more accurate analysis of the diode quality of the cell which can be used as an indicator of enhanced recombination due to Cu defect formation in or close to the space-charge region. It has been proposed that this method can be used to predict cell lifetime under field conditions, with sufficient long-term reliability of plated cells having been demonstrated in several studies [14–17]. However, the Suns-V_{OC} technique [18] which is used to extract *pFF* values can be influenced by properties of the contact such as contact resistance, and poor contact material integrity can result in non-ohmic behaviour which can lead to errors in extracted diode parameters. The possibility of degraded contact integrity in these tests has major implications for the accuracy of

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long-term reliability tests using this method, as minor errors in degradation measurements can have large impacts on the estimated lifetime of plated cells [13].

In this study, silicon solar cells with plated Ni/Cu/Ag stacks underwent thermal stress testing to assess the material integrity of the contacts and the electrical properties of the cells after extended exposure to elevated temperatures. A combination of electrical and material characterisation techniques were used to investigate changes in contact structure and analyse the influence of changes in that structure after thermal stress testing on extracted diode parameters via Suns-V_{OC} measurements. Insights were gained into the impact of cell metallisation degradation on the analysis and assessment of long-term reliability via Arrhenius modelling. The study also highlights the propensity of Cu to diffuse through polycrystalline metals at relatively low temperatures and therefore raises further concerns about Cu diffusing through Ni barrier layers and penetrating the silicon of the cell.

2. Experimental

2.1. Sample preparation and thermal stress testing

Cells were fabricated using 156 mm boron-doped 1–3 Ω cm Czochralski (Cz) silicon wafers with random-pyramid texturing. A phosphorus-doped emitter with a sheet resistivity ~110–120 Ω/□, surface concentration of ~2 × 10^{19} cm^{-3} and junction depth of ~0.4 µm was formed using $POCl_3$ diffusion. After rear etching, a 75 nm silicon nitride (SiN_x) anti-reflection coating was deposited using direct plasma enhanced chemical vapour deposition (PECVD) and a full-area aluminium rear contact was screen-printed and fired to form a full-area back surface field (BSF).

Small cell contact grids (25 mm × 25 mm cell area) were patterned on the front surface using a 266 nm ps Lumera Super Rapid Nd: YAG laser with a BBO crystal for the 4th harmonic, with an average laser fluence of 0.44 J/cm^2 and 37% pulse overlap being used to form both the fingers and busbars. The ablated finger width was 13 µm and a finger spacing of 1.5 mm (16 fingers in total) was used to form the metal grids via stage scanning. Busbars 1 mm-wide were ablated with a 9 µm pitch between adjacent laser scans using stage scanning. After removal of the native oxide by immersion of the front surface in 1% (w/v) hydrofluoric acid (HF), front contacts were formed on the exposed Si by plating a stack of Ni (~1 µm) and Cu (8–10 µm) using bias-assisted light induced plating (LIP) with Barrett SN1 Ni sulphamate (MacDermid Inc.) and Helios EP2 Cu (MacDermid Inc.) plating solutions, respectively. Bias currents of 23 mA/cm^2 and 40 mA/cm^2 were used for Ni and Cu LIP, respectively.

Two different capping methods were used – Ag capping with bias-assisted LIP (MacDermid Helios Silver EPF 400), and capping with a Ag immersion solution (MacDermid Helios Silver IM 452). The average thicknesses of the capping metals were ~1.0 µm and ~0.3 µm respectively. Each 156 mm cell precursor contained 25 small cells, so individual cells were laser cleaved after plating for edge isolation, characterisation and further processing. Some samples were sintered in a rapid thermal processing (RTP) furnace at 350 °C for 1 min in N_2 ambient before characterisation, whilst other samples were characterised without sintering. One cell from each set was used as a control for contact characterisation and did not undergo thermal stress testing. Cells were exposed to 200 °C in a muffle oven with N_2 ambient for 500 h to simulate long-term operation at elevated temperatures.

After thermal annealing at 200 °C, some cells were quenched in ethylene glycol (cooling rate ~1000 K/s) immediately after thermal treatment followed by rinsing in DI water while the remaining cells were cooled under ambient conditions (cooling rate ∼4 K/s). The different quenching methods were examined because Flynn et al. [19] had previously shown that quenching after thermal annealing of laser-doped Ni/Cu-plated cells can result in the formation of Cu precipitates close to the laser-doped surface and reduce photoluminescent imaging intensity, whereas no Cu precipitates were able to be detected with slow cooling. The impact of cooling rate on Cu out-diffusion and precipitation in Si has also been observed in several other studies [20,21]. This study aimed to see whether the quenching process contributed to any changes in the contact integrity after thermal annealing.

2.2. Cell characterisation

Cells were electrically characterised before and after thermal exposure using a combination of light and dark *I-V* measurements using a calibrated in-house constant illumination *I-V* tester under standard test conditions. Suns-V_{OC} measurements were performed using a Sinton Instruments Illumination-voltage tester, with Suns-V_{OC} being measured at three points along the 25 mm long busbar (one at each end of the busbar and one in the centre). Characterisation of the contact structure at regions of interest was performed by obtaining cross-sections using single beam focussed ion beam (FIB) milling (FEI XP200), followed by high-resolution imaging of the contact cross-section. Transmission electron microscope (TEM) specimens were then prepared using the FEI XP200 and TEM imaging was performed with a Philips CM200 TEM system. Energy dispersive X-ray Spectroscopy (EDS) measurements were obtained with a Bruker SDD detector.

3. Results and discussion

The first indication of thermally-induced contact damage impacting plated cell characterisation can be observed in the Suns-V_{OC} curve in Fig. 1. This response was measured for a Cu-plated cell with a LIP Ag capping layer that had been annealed at 200 °C for 500 h with the reversal in the open-circuit voltage (V_{OC}) occurring at illumination intensities greater than ~2 Suns. This V_{OC} 'bend-back' can indicate the presence of a Schottky barrier between the probe and the Si, the diode resulting in an opposing voltage to the cell junction voltage at high illumination intensities. This phenomenon has been previously described [18,22,23], usually in relation to rear point contacts. It has also been reported for plated laser-doped bifacial cells, where insufficient p-type dopants were incorporated at the laser-doped contacts [24].

Contacts can be modelled as a Schottky diode in parallel with a shunt resistance, the latter representing the contact resistance of the metal to the Si as depicted in Fig. 2. At a well-formed contact, the Schottky diode is bypassed by the shunt resistance and no voltage exists over the diode at the metal-Si interface. However, if the contact between the probe and Si is highly resistive, then at illumination intensities above normal operating conditions, current cannot be

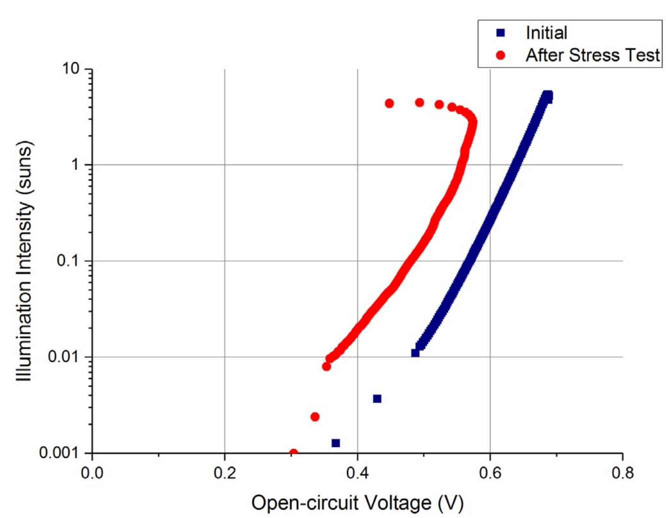

Fig. 1. Suns-V_{OC} curve measured on a Cu-plated solar cell with a LIP Ag capping layer (sintered) before and after thermal exposure at 200 °C for 500 h.