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TiO_2 as intermediate buffer layer in $Cu(In,Ga)Se_2$ solar cells

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ABSTRACT

The application of TiO_2 as part of the buffer layer stack in thin film $Cu(In,Ga)Se_2$ (CIGS) solar cells is investigated for the improvement of the photovoltaic device performance. In a standard device configuration a CdS/ZnO/Al:ZnO layer stack is applied onto the CIGS absorber layer. By decreasing the CdS buffer layer thickness a higher photocurrent is expected from a reduced parasitic absorption. When the CdS layer is not fully covering the CIGS surface, losses in V_{OC} and FF are observed in I-V measurements due to the arising unfavorable CIGS/ZnO band alignment and sputter damage on the CIGS surface. Here we present thin TiO_2 layers deposited by atomic layer deposition at low temperature as alternative to the unintentionally doped ZnO. With this approach, the photocurrent can be increased without adversely affecting V_{OC}. Comparable device efficiency is achieved for the investigated structure and the reference process with the gain in current density being compensated by increased series resistance. Temperature dependent I-V measurements coupled with 1D-SCAPS simulations suggest a positive conduction band offset at the CdS/TiO_2 interface limiting the FF. ALD-TiO_2 is suggested as a more suitable intermediate buffer layer than sputtered ZnO when thin CdS buffer layers are applied.

1. Introduction

Solar cells based on chalcopyrite $Cu(In,Ga)Se_2$ (CIGS) absorbers are among the most promising thin-film photovoltaic technologies with laboratory scale power conversion efficiencies (PCE) reaching 20.4% on a flexible polymer substrate [1] and 22.6% on a soda lime glass (SLG) substrate [2]. CdS grown by chemical bath deposition (CBD) is commonly employed as a buffer layer in CIGS solar cells enabling the aforementioned champion device efficiencies. The relatively low band-gap energy of CdS (2.4–2.5 eV), however, limits the optimum performance of the cells due to parasitic absorption in the short wavelength region [3].

In order to reduce this parasitic absorption several approaches have been proposed by applying alternative buffer layers with a wider bandgap and/or lower absorption coefficient such as Zn(S,O,OH), $Zn_{1-x}Sn_xO_y$, In_xS_y and $Zn_xMg_{1-x}O$ achieving a PCE of 21.0% [4], 18.2% [5], 18.2% [6] and 18.1% [7], respectively. Amorphous TiO_2 has also been reported to work as a buffer layer on a non-vacuum deposited CIGS absorber but with limited PCE of 9.9% for a cell with active area of 10.5 mm^2 [8].

Another approach to minimize the optical losses is the reduction of the CdS layer thickness. It has been reported that a minimal thickness of about 50 nm is necessary for optimal performance in CIGS cells without an alkaline post deposition treatment (PDT) [9,10]. The application of KF PDT allowed for a reduction of the CdS thickness down to about 30 nm [1]. A further thickness reduction, however, leads to a non-uniform coverage of the CIGS surface and severe degradation of the current-voltage (I-V) parameters V_{OC} and FF [11]. This is supposed to stem from a cliff-like band alignment and thus carrier recombination at the CIGS/ZnO interface [12–14] and sputter damage on the CIGS surface from the subsequent ZnO/Al:ZnO window layer deposition [14–16]. The application of a thin Al_2O_3 layer deposited by atomic layer deposition (ALD) on top of CBD-CdS was reported to partially mitigate the losses in V_{OC} and FF for CdS layers thinner than 30 nm. The thickness constraint to about 1 nm of the highly resistive Al_2O_3, however, sets a limit to the achievable V_{OC} recovery [11].

A different approach was taken by Kobayashi et al. [15] by successfully replacing the sputtered Al:ZnO window layer with B:ZnO deposited by metal-organic chemical vapor deposition (MOCVD) when a thin (10 nm) Zn(S,O,OH) buffer layer was used. The work of Minemoto and Julayhi focused on optimizing the band-alignment with a sputtered $Al:ZnO_{1-x}S_x$ window layer in a buffer-less CIGS cell concluding that the inferior conversion efficiency is due to sputter damage on the CIGS surface [16]. What is not considered with this approach are further beneficial effects of a buffer layer: e.g. a possible buried junction, positioning of the interface Fermi level close to the absorber conduction band and surface inversion, mitigating harmful defects (see [3,17]).

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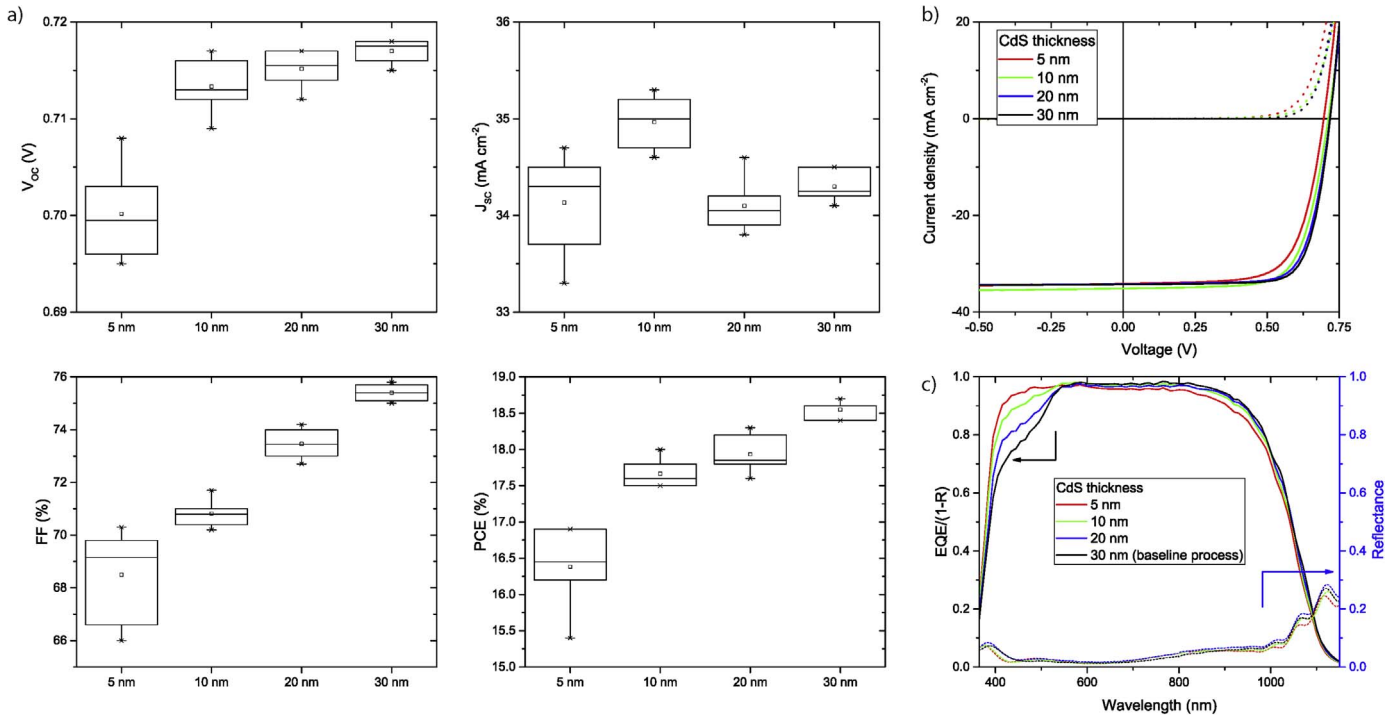

Fig. 1. a) Boxplot chart (6 best performing cells of each sample) of the current-voltage parameters of a baseline structure SLG/Mo/CIGS/CdS/ZnO/Al:ZnO/grid(Ni,Al)/MgF_2 with varying CdS buffer layer thickness from ~ 5–30 nm. b,c) corresponding J-V curves, internal quantum efficiency and reflectance measurement of representative cells.

In this contribution a thin CdS layer is combined with an ALD-TiO_2 to constitute the interlayer structure between the CIGS absorber and Al:ZnO front contact. With this approach the CIGS/CdS interface and band-alignment is maintained while the CIGS/ZnO interface is avoided in case of insufficient CdS coverage. Furthermore TiO_2 is replacing ZnO as highly transparent and resistive (HTR) layer in its function of preventing electrical inhomogeneities and shunt paths [18,19]. The soft deposition method thermal-ALD is selected to mitigate sputtering damage on the CIGS surface and for a precise thickness control of the deposited TiO_2.

2. Experimental section

2.1. Sample fabrication

The architecture of the multilayer device under investigation is SLG/SiO_2/Mo/CIGS/CdS/HTR/Al:ZnO/MgF_2 where the baseline unintentionally doped ZnO HTR layer is replaced with TiO_2.

The CIGS absorber layers were deposited on SiO_2 and Mo coated soda lime glass (SLG) substrates by elemental co-evaporation from effusion cells at a base pressure of ~ 10^{-5} Pa in a multi-stage process as reported before [20]. Additionally a NaF and RbF PDT was performed. The absorber layer composition was measured by x-ray fluorescence giving a [Cu]/([In] + [Ga]) ratio of 0.83–0.86 and a [Ga]/([Ga] + [In]) ratio of 0.44–0.46. An absorber layer thickness of 3 µm was determined by scanning electron microscopy (SEM).

The CdS buffer layer was deposited by CBD from a bath of cadmium acetate (2.1 mM), thiourea (22 mM) and ammonium hydroxide (2 M [NH_3]) at 70 °C. The thickness was controlled by the time the sample was immersed in the bath. After the deposition a short annealing (2 min) at 180 °C and ambient atmosphere was performed. The thickness of CdS was determined by SEM for layers with a thickness above 20 nm. For thinner layers the thickness was estimated by reproducing the CdS absorption in the blue region of the EQE measurements using as input the extinction coefficient of CdS.

For the reference structure ~ 60 nm ZnO was deposited by rf-magnetron sputtering in an Ar/O_2 (0.02%) atmosphere at a pressure of 0.46 Pa and a power density of 1.9 W cm^{-2}. The alternative HTR layer TiO_2 was deposited by ALD at a substrate temperature of 100 °C from tetrakis(dimethylamino)titanium(IV) (TDMAT) and H_2O with a Fiji G2 system (Ultratech). Ar was used as carrier gas at a base pressure of 28 Pa. The source temperature of TDMAT was at 75 °C while H_2O was kept at room temperature. A saturated growth of 53 ± 0.2 pm/cycle was determined by ellipsometry on Si (100) reference substrates for the ALD cycle of H_2O/Ar purge/TDMAT/Ar purge using pulse lengths of 0.06/65/0.6/65 s, respectively. SEM micrographs of TiO_2 on CIGS or on CIGS/CdS showed a comparable growth rate with a larger uncertainty. No post deposition annealing was performed on the TiO_2 layer which is therefore assumed to be amorphous as reported for comparable deposition conditions [21–23].

The cells were finished with a sputtered ~ 260 nm Al:ZnO (2%$_{at}$ Al, 1.8 W cm^{-2}), 105 nm of MgF_2 and 4 µm Ni/Al grid by e-beam evaporation. Mechanical scribing was used to define a cell area of 0.25 ± 0.02 cm^2.

2.2. Characterization methods

I-V curves were measured with a Keithley 2400 source meter and four-terminal sensing under standard test conditions (1000 W m^{-2}, 298 K) using a type ABA solar simulator. Temperature dependent measurements were performed in a cryostat with liquid nitrogen cooling and a halogen lamp. External quantum efficiency (EQE) measurements were performed with a chopped white light source (halogen), a tripple-grating monochromator and a lock-in amplifier under ~ 100 W m^{-2} white light bias at 298 K. A monocrystalline Si solar cell certified by Fraunhofer ISE was used as a reference. The internal quantum efficiency (IQE) was calculated with EQE/(1-R) where R denotes the reflectance. Reflectance measurements were performed on a Shimadzu UV-3600 spectrophotometer. SEM was performed on a Hitachi S-4800 electron microscope.

3. Results and discussion

The effect of reducing the CdS buffer layer thickness on the cell