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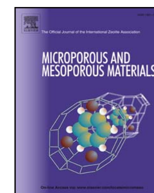

Integration of thin film of metal-organic frameworks in metal-insulator-semiconductor capacitor structures

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ABSTRACT

Integrating nanoporous metal-organic frameworks, MOFs, in electrical devices enables various applications, for instance, as sensor or memristor. The incorporation of thin MOF films in metal-insulator-semiconductor, MIS, capacitor structures is particularly attractive, since its operation at low voltages enables real-life applications. Here, thin $Cu_3(BTC)_2$, also referred to as HKUST-1, MOF films were deposited on thermally grown silicon dioxide surfaces in a layer-by-layer fashion. A peak of the conductance is observed, an evidence for interface states. Temperature dependent measurements reveal the formation of a counter clockwise hysteresis, due to charge injection mechanism. Finally, capacitance and conductance in strong accumulation decrease as the sample is heated slowly up to 100 °C. The cooling process results in a reverse process. Capacitance-voltage and conductance-voltage characteristics, measured in forward and reverse direction at different applied frequencies and temperatures, show the high quality of the interfaces which makes them suitable for advanced sensing and electronic applications.

1. Introduction

Metal-organic frameworks (MOFs) are nanoporous, crystalline solids composed of metal nodes connected by organic linker molecules. Their incorporation in electronic devices have been emerged as promising candidates for sensing applications due to its tailorable chemistry nature, by adapting the functionality of its components [1,2]. Further properties making them perfectly suited for sensing application are their large surface areas, their tunable porosities, the low dielectric constants and their high selectivity towards specific molecules [3–5]. The sensing of guest molecules was demonstrated by measuring the change in luminescence intensity, impedance, mass uptake and interference peaks [6–9]. Several deposition techniques were developed to achieve MOF sensors. In addition to the common, solvothermal synthesis, many other approaches were realized to prepared MOF materials on substrates [10–12]. For instance, the chemical vapor deposition has emerged as a promising free solvent growth [13]. By controlled layer-by-layer synthesis, resulting in surface-mounted MOFs, also referred to as SURMOFs, the layer thickness was considerably reduced [14]. Although significant progress has been made on the growth of thin MOF films, only a few reports address the integration of MOFs in electronic devices. For example, Wu et al. fabricated the first microporous field-effect transistor (FET), using $Ni_3(HiTP)_2$ as an active channel material and obtained a high charge mobility [15]. Gu et al. improved the performance of an OFET by using $Cu_3(BTC)_2$ in order to modify the silicon dioxide dielectric layer [16].

Generally, a large number of MOFs with good sensing characteristics are available [2]. In particular, $Cu_3(BTC)_2$ (BTC = 1,3,5 benzenetricarboxylate) [17], also referred to as HKUST-1, has excellent properties such as its rigid structure under post-annealing treatments and a low dielectric constant of (k = 1.7) [18]. In addition, it was demonstrated that $Cu_3(BTC)_2$ can be grown on silicon dioxide surfaces with a low surface roughness and high structural quality [19,20]. The $Cu_3(BTC)_2$ SURMOFs are usually grown as crack-free and defect-free films [21]. These characteristics are prerequisites for the implementation of MOFs in metal insulator semiconductor, MIS, capacitors.

In this work, we present the fabrication of conventional MIS capacitors using $Cu_3(BTC)_2$ MOF as insulating material. Thin $Cu_3(BTC)_2$ films were prepared in a layer-by-layer fashion by dip-coating using a dipping robot equipped with ultrasonication [20]. More details for the layer-by-layer SURMOF synthesis can be found in Ref. [14,22]. The influence of the interface states as well as the charge mechanisms was evaluated through capacitance voltage (*C-v*) and conductance voltage (*G-V*) characteristics. The major benefit in comparison to the already

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reported MOF-based-FET electronic devices, which require relatively high voltages, is that the MOF-MIS-device can be operated with less than 10 V. The low-voltage-operation and thus the low-energy-consumption could enable real-life applications.

2. Experimental

$Cu_3(BTC)_2$-MOF-based MIS capacitors were fabricated on boron doped p-type silicon (p-Si) wafer with a (100)-orientation, 500 μm thickness and 0.5–0.75 Ωcm resistivity. First, 10 nm silicon dioxide (SiO_2) was thermally grown. The thickness of the oxide layer was verified by ellipsometry. Second, Al contacts were deposited on the back side of the wafer. Third, the oxide surface was coated by $Cu_3(BTC)_2$ SURMOFs in a layer-by-layer process in 15 dipping cycles. Finally, 100 nm thick circular Al gate contacts with an area of 0.0061 cm^2 were evaporated through a shadow mask.

The *C-V* and *G-V* characteristics of the p-Si/SiO_2/$Cu_3(BTC)_2$/Al structure were examined using an Agilent 4294A impedance analyzer. The measurements were conducted with a small AC signal of 25 mV and by sweeping the DC gate voltage (at the p-Si substrate) from − 6 to 4 V. Frequency dependence measurements were carried out in the frequency range 1–100 kHz at room temperature (RT). Temperature dependent measurements were conducted in the temperature range of 30–100 °C at 100 kHz.

3. Results

The crystalline structure of SURMOF thin film on the MIS capacitor was investigated by X-ray diffraction (XRD) experiments, Fig. S1. The XRD patterns verify the crystalline structure of the $Cu_3(BTC)_2$ film, which is mainly grown in (222) orientation to the substrate. Atomic force microscopy measurements show a smooth surface morphology, Fig. 2S. The root mean square was 11.6 nm in 1 μm × 1 μm and 15.3 nm in 5 μm × 5 μm.

3.1. Frequency dependence of C-V and G-V

Capacitance-voltage, *C-V*, and conductance-voltage, *G-V*, characteristics of p-Si/SiO_2/$Cu_3(BTC)_2$/Al capacitor structure measured at 500 kHz at room temperature are shown in Fig. 1. Both curves exhibit the three characteristics regimes of accumulation, depletion and inversion typical for a functional capacitor [23]. There is also a small deviation of the reverse capacitance and conductance measurements. This suggests the existence of small fixed charges in the MOF [24]. In addition, the conductance gives a peak in depletion as a signature of interface states. The reproducibility of the capacitance and conductance behavior were evaluated by performing several measurements in different positions of the device with 2 cm × 2 cm dimensions and also in contacts with different areas (Fig. 3S). The results demonstrate a good homogeneity of the MOF with only a small deviation in the accumulation capacitance.

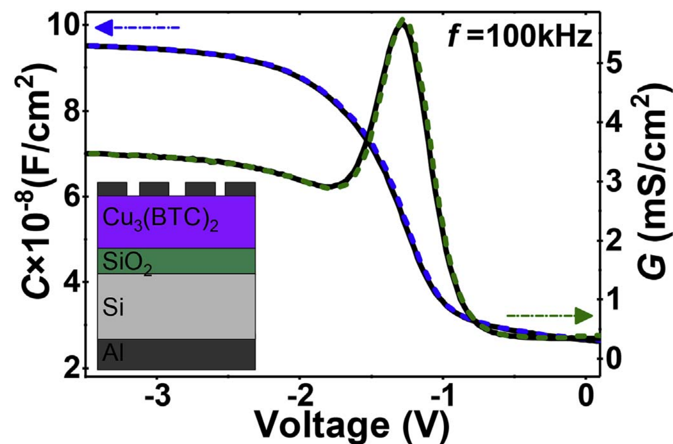

Fig. 1. Capacitance-voltage, conductance-voltage and device structure of p-Si/SiO_2/$Cu_3(BTC)_2$/Al MIS capacitor structure measured from forward (solid line) to reverse (dotted line). The inserted graphic shows a schematic representation of the device structure.

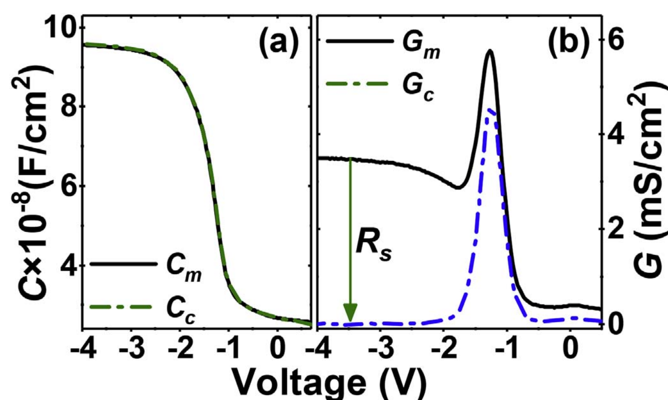

Fig. 2. Corrected (solid line) and non-corrected (dash line) capacitance (a) and conductance (b) voltage characteristics of p-Si/SiO2/Cu3(BTC)2/Al MIS capacitor structure measured at 100 kHz.

The electric characteristics of a MIS capacitor are mainly affected by series resistance (R_s) and interface states. The effect of the series resistance was subtracted from the measured capacitance (C_m) and conductance (G_m) in strong accumulation using the factor correction developed by Nicollian [25]. This results in the corrected capacitance (C_c) and corrected equivalent parallel conductance (G_c). The effect of series resistance is shown in Fig. 2. Capacitance curve is not influenced by R_s. In contrast, the conductance values are shifted toward lower values, especially in accumulation and depletion.

Fig. 3 shows the parallel conductance versus voltage bias measured in the frequency range from 1 to 500 kHz. The obtained series resistances were between 0.22 and 120.1 Ωcm^2. An increment of the conductance peak with the frequency is observed because of the contribution of the surface states [26]. The maximum peak position of the parallel conductance is shifted to lower voltages as the frequency decreases. This behavior is attributed due to the different time responses of interface states [27].

3.2. Temperature dependence of C-V

Heating experiments were performed to desorb guest molecules

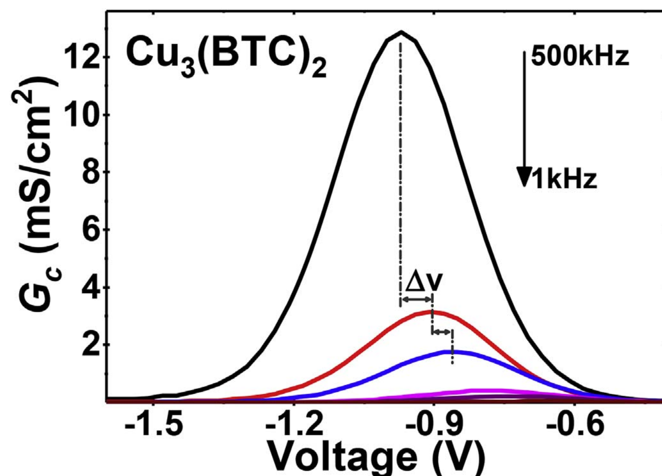

Fig. 3. Parallel conductance-voltage characteristics of p-Si/SiO2/Cu3(BTC)2/Al MIS capacitor structure measure at different frequencies.

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