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First prototype of high-speed data acquisition system of ion source for neutral beam injection on EAST

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ABSTRACT

The ion source is the critical part of Experimental Advanced Superconducting Tokamak (EAST) neutral beam injection (NBI) system. Two ion sources are equipped in one beam line. The voltage and current signals of grids are the important diagnostic data in the duration of beam extraction, especially the rising and sparking edge. In order to achieve the functions of data acquisition and isolation transmission, the first prototype of high-speed data acquisition system of ion source has been developed. The system contains the advantages of 40 MS/s sampling rate, 8-bits resolution and optical isolation transmission. Field programmable gate array (FPGA) is used as the control chip in the system. The system has been tested for the voltage of plasma grid (PG) and the beam current. The error range of system is < 3% after the test. These results present that the data acquisition system is promising equipment for NBI.

1. Introduction

Two beam lines of NBI system have been developed at the Institute of Plasma Physics, Chinese Academy of Sciences (ASIPP). In order to support the physical experiment of EAST, NBI systems own the capacity of 4–8 MW beam power with 10–100 s [1–3].

In NBI system, many kinds of electrical and physical parameters need to be measured for analyzing the system operational state and the power of injection. The voltage and current signals of ion source grids are the critical parameters for physical analysis. Pulse Step Modulator (PSM) technology is used in accelerator power supply, and the on-state time of one modulator is 1–5 μs [4]. So, the high-speed data acquisition system based on FPGA EP4CE6E22C8N should possess the enough sampling rate to acquire the rising edge of modulator. In order to ensure the data transmission precision, optical isolation transmission is adopted in the system. Meanwhile, the experimental shots should be saved by PXI platform and displayed in LabVIEW software [5]. In view of the above requirements, the first prototype of high-speed data acquisition system has been developed. Analog signal reinstitution is realized by the high-speed data acquisition system.

The details of high-speed data acquisition system based on FPGA are described in the following parts. In part 2, the architecture of the system is described, part 3 shows the experimental results. At last, part 4 gives the conclusion.

2. Hardware architecture of system

As shown in Fig. 1, the high-speed data acquisition system consists of HV voltage divider, current sensor, transmission circuit board, reception circuit board, and PXI platform.

The power supply of PG contains 144 modulators, and the voltage of one modulator is 780 V. In order to measure the high voltage, the HV voltage divider is necessary. The ROSS HV voltage divider adopted in the system has the characteristic of input resistance is 1 MΩ. And the HV voltage divider is parallel connection to plasma grids of ion source. The output of HV voltage divider is 0–10 V that matches with 0–100 kV. Considering the negative power supply of suppressor grid (SG), the input range of transmission circuit board is designed for −10 to 10 V. The PEARSON 101 [6] current sensor is used in the system, and the output voltage of sensor per ampere is changed to 1/30 V/A, which is suited to be acquired by high-speed data acquisition system.

Because of the complicated electric and magnetic field environment of experimental hall, the acquisition data is not suitable for long-distance transmission. Considering the factor, the data acquisition system must have the ability of optical isolation transmission. So, the transmission circuit board converts the sampling voltage into optical signal that is transmitted to reception circuit board by optical fiber. It presents the galvanic isolation and the immunity to Electro-Magnetic Interference (EMI).

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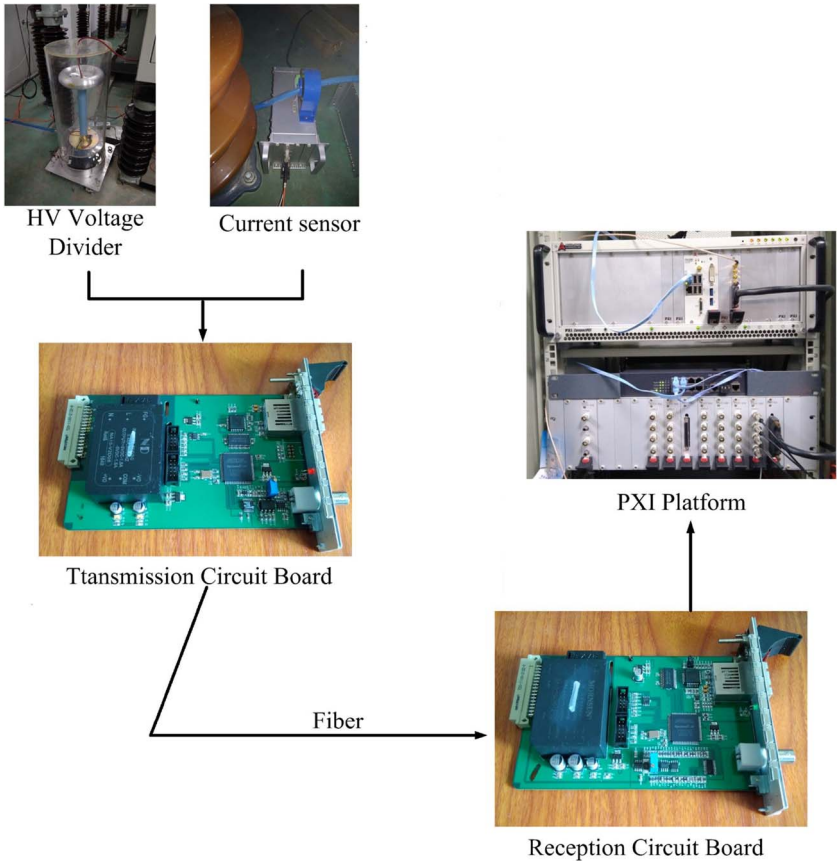

Fig. 1. The hardware architecture of high-speed data acquisition system.

Reception circuit board receives the optical signal, and then converts it to analog signal. The output of reception circuit board is −10 to 10 V that matches with the input of transmission circuit board.

The analog signal from reception circuit board is acquired and saved by PXI platform, and also recalled by Labview [7], which is convenient for the next phase of analysis. Individual circuit boards indicated in Fig. 1 have been described in the following parts.

2.1. Hardware of transmission circuit board

The section describes the components of transmission circuit board, such as voltage regulation circuit, analog-to-digital (AD) conversion circuit, FPGA, CY7B923 [8] circuit and optical isolation circuit. The structure diagram of transmission circuit board is shown in Fig. 2. In order to satisfy the input range of AD chip AD9057 [9], voltage regulation circuit converts the input voltage −10 to 10 V to 2–3 V. Then the AD chip converts input voltage to 8-bits digital codes that are acquired by FPGA. In the CY7B923 circuit, the 8-bits digital codes are encoded to serial data. Meanwhile, the serial data are transmitted by fiber optical transceivers HFBR-53D5 [10] with multimode fiber-optic cables. The crystal oscillator 40 MHz is the synchronous signal in transmission circuit board. The flash chip is used for loading program of FPGA [11]. The individual components of transmission circuit boards are indicated as following:

FPGA receives the CLK signal from crystal, and then sends the synchronous clock signals to CY7B923 and AD9057. In the rising edge of CLK, FPGA acquires the output of AD9057. In the next rising edge of CLK, FPGA enables the data select pin of CY7B923 and sends the acquired 8-bit data to CY7B923.

As shown in Fig. 3, the voltage regulation circuit achieves the function of voltage conversion. R_4 is the feedback resistance of amplifier. R_1, R_2, and R_3 are the input resistances of AD8065 FastFET amplifiers that are voltage feedback amplifiers with FET inputs offering high performance and ease of use. V_1 is the input voltage of positive input end of amplifier [12]. The negative input end of amplifier is V_2. The output voltage V_o is connected to AD chip AD9057 which input voltage is 2–3 V. V_o is calculated by Eq. (1).

$$Vo = \frac{R_3}{R_1 + R_3}\frac{R_2 + R_4}{R_2}V_1 - \frac{R_4}{R_2}V_2 \quad (1)$$

Considering the output of V_o is 2–3 V, V_2 is set at median −2.5 V. So, in Eq. (1), the coefficient of V_2 is 1. Let $R_4 = R_1 = 1$ kΩ. Because the input range of voltage regulation circuit is −10 to 10 V, and the input voltage difference of AD9057 is 0–1 V. The coefficient of V_1 is set as 1/20 in Eq. (1). Then we can calculate the $R_3/(R_1 + R_3) = 1/40$ [13,14]. Considering the input bias current of AD8065, the ideal result is $R_1 = 39$ kΩ, $R_3 = 1$ kΩ. In order to reduce the influence of AD8065's bias current, the inverting amplification circuit based on TL072 is adopted in the system. The center voltage 2.5 V of V_o can be adjusted by R_6.

As discussed in above section, the converted voltage is connected to the input end of AD chip AD9057. Because of a 40 MHz encode rates and full-power analog bandwidth of 120 MHz, the perfect dynamic performance of the chip is ideal for design. The 8-bit data generated by AD9057 is acquired by FPGA synchronously. In order to analyze the operational state of difference amplifier circuit and FPGA, the SignalTap II logic analyzer software [15] is used for monitoring the input signal. In Fig. 4, the digital codes acquired by FPGA are shown in SignalTap II. AD_DATA [0] ~ AD_DATA [7] are the digital codes converted by AD9057. SignalTap II integrated the digital codes into analog signal wave that is shown in Fig. 4. According to the analog signal wave and the digital codes, we can analyze the input signal and the running status of sampling circuit of transmission circuit board.

After acquiring the digital codes, FPGA sent them to optical