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Energy efficient implementation of multi-phase quasi-adiabatic Cyclic Redundancy Check in near field communication

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ABSTRACT

Ultra-low power operation in power-limited portable devices (e.g. cell phone and smartcard) is paramount. Existing conventional CMOS consume high energy. The adiabatic logic technique has the potential of rendering energy efficient operation. In this paper, a multi-phase quasi-adiabatic implementation of 16-bit Cyclic Redundancy Check (CRC) is proposed, compliant with the ISO/IEC-14443 standard for contactless smart cards. In terms of a number of CRC bits, the design is scalable and all generator polynomials and initial load values can be accommodated. The CRC design is used as a vehicle to evaluate a range of adiabatic logic styles and power-clock strategies. The effects of voltage scaling and variations in Process-Voltage-Temperature (PVT) are also investigated providing an insight into the robustness of adiabatic logic styles. PFAL and IECRL designs using a 4-phase power-clock are shown to be both the most energy-efficient and robust designs.

1. Introduction

CRC is widely used in all data-communication, transmission and memory devices as a powerful method for detecting errors. One of the traditional hardware solutions for the CRC calculation is a bit-serial approach using a Linear Feedback Shift Register (LFSR), consisting of XOR gates and flip-flops [1]. A general diagram for CRC using an LFSR is shown in Fig. 1. Depending on the application, a generator polynomial is used which gives a high probability of error detection [2]. For very high-speed data transmission, researchers have proposed many hardware and software-based CRC implementations. These include parallel software implementations based on look-up algorithms [3] and hardware implementations based on the z-transform [4], matrix formulation [5] and pipelining [6]. These parallel approaches focus mainly on fast error detection when processing large data messages. Software solutions have several drawbacks: they are slow, they occupy processor resources, and require ROM storage for the lookup table. Nevertheless, in the references cited above, the energy consumption has not been considered.

1.1. Motivation

Due to the increased usage of battery-less applications (e.g. a smartcard) and rising energy density due to the technology shrinkage, energy-efficiency has become a major concern in the design of large systems. To address this, a circuit technique, "Quasi-Adiabatic Logic" based on the CMOS technology, has the potential for low energy operation albeit at some cost in terms of performance speed. However, adiabatic logic can provide sufficient performance to be used to design energy-efficient communication protocol which has low data rate such as Radio Frequency Identification (RFID) and NFC operating at 13.56 MHz. Although, adiabatic logic is in existence for more than two decades, still, its full potential has not been discovered.

In the literature, researchers have mostly demonstrated the low energy benefits of adiabatic logic using implementations such as counters [7], multiplexers, adders and multipliers [8]. At the system level, very few papers exist [9,10], demonstrating the energy benefits in comparison to non-adiabatic (static CMOS). In this paper, we compare the performance of multi-phase adiabatic logic designs in particular energy dissipation, throughput, latency, area, robustness and complexity based on the circuit and the power-clocking scheme. Practically, it is difficult to design an optimum adiabatic system but the trade-offs between energy, speed, area, complexity and robustness can be established that enables the designer to design an optimum adiabatic logic system. The main motivation of this work is to design an energy-efficient 16-bit CRC based on the standards and protocol of the NFC frame format outlined in ISO/IEC 14443-3 [11,34].

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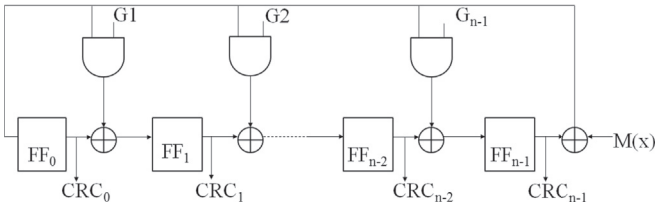

Fig. 1. A bitwise serial LFSR for n-bit CRC generator.

1.2. Contribution of this paper

The focus of this paper is to compare a CRC implemented using five energy-efficient quasi-adiabatic logic designs namely: Efficient Adiabatic Charge Recovery Logic (EACRL), Improved Efficient Charge Recovery Logic (IECRL), Positive Feedback Adiabatic Logic (PFAL), Complementary Pass-transistor Adiabatic Logic (CPAL) and Clocked Adiabatic Logic (CAL) and analyse the performance trade-offs over a wide range of external constraints as discussed above. Here the multi-phase is referred to as the power-clocking scheme used by adiabatic logic designs. The main contributions of this paper are numbered as follows;

1) We present a hardware implementation of 16-bit multi-phase adiabatic CRC for NFC application.
2) We present a CRC design which can be scaled up or down by adding or removing the CRC slices in the datapath and flip-flops in the register unit for an application other than the NFC.
3) A methodology is proposed to minimize the design time and synchronisation issue by implementing a CRC design which is suitable for a range of adiabatic clocking strategies, specifically 4-phase, 2-phase and single phase.
4) A system level implementation of CRC comprises of a power-clock generator for different adiabatic clocking strategy was implemented and compared on the basis of energy consumption.
5) Finally, we analyse the performance trade-offs in terms of energy benefits, throughput, latency, complexity, robustness and area between multi-phase adiabatic CRC implementations. We also compare these with a non-adiabatic CMOS design.

1.3. Structure of the paper

The structure of the paper is as follows. Section 2 reviews the energy dissipation of the quasi-adiabatic logic due to adiabatic loss and non-adiabatic losses. Then the five chosen quasi-adiabatic logic techniques are discussed in short. Section 3 presents the application of CRC in NFC. The design methodology is presented in Section 4. Implementations of 16-bit CRC according to ISO/IEC 14443 standard are presented in section 5. Section 6 presents the simulation results and performance comparison using five adiabatic logic designs and non-adiabatic logic design. Finally, the paper is concluded in section 7.

2. Quasi-adiabatic logic families

The term "Quasi" describes the logic that involves some theoretical losses arising due to the threshold voltage degradation. Such losses are termed as Non-Adiabatic Loss (NAL). For low energy operation, adiabatic logic uses a slowly changing power-clock which allows approximately constant current charging/discharging and by avoiding current surges, the circuit dissipates less energy [12]. In addition, the power-clock also makes possible the recovery of charge by pumping the stored energy back to the power supply during the discharging process. The power-clock generator can be implemented either using a stepwise charging circuit [13,14] or an inductor based generator [15,16]. For more than two decades, adiabatic logic has been widely studied and various energy efficient logic families have been proposed [7–10]. Since the implementation and the distribution of multiphase power-clocking scheme requires additional area, energy consumption and increases complexity, logic families with more than 4-phases are not taken into account.

Single-phase and 4-phase power-clocks are broken down into four equal time periods namely evaluation (E), hold (H), recovery (R) and idle (I). On the other hand, due to the non-overlapping power-clock requirement of 2-phase, its idle time period is three times than the rest of each three time periods. Fig. 2 shows the corresponding multi-phase power-clocking schemes along with the relationship of the power-clock period, $T_{clk,\ phase}$, with the ramping time, T_r.

The mathematical relationship for the energy dissipation also known as adiabatic loss (AL), E_D, using a ramp during charging phase is given as;

$$E_D = \frac{R_{ON} C_L}{T_r} C_L V_{DD}^2 \tag{1}$$

Where C_L is the lumped load capacitance at the output node of the circuit, R_{ON} is the resistance of the charging path and V_{DD} is the maximum supply voltage. The detailed derivation of (1) is given in Ref. [17]. According to (1), it is possible to reduce the energy dissipation to an arbitrary degree by increasing the ramping time to ever-larger values. However, there is a practical lower limit to the ramping time value due to the increased leakage at longer ramping times.

These adiabatic logic families also suffer from NAL arising in the evaluation and recovery phase depending upon the circuit topology. NAL occurs because of the threshold voltage degradation. In the evaluation phase, the output follows the power-clock only when the source-to-gate voltage of pMOS transistor is greater than or equal to its threshold voltage $|V_{t,p}|$. Similarly, during the recovery phase of the power-clock, when the supply voltage goes below the threshold voltage, through one of the pMOS transistors, it is turned off and a residual charge remains on the output node. This residual charge gets discharged non-adiabatically at the start of the next cycle when new input is evaluated. This part of non-adiabatic discharge is independent of the frequency but can cause high energy dissipation for large system designs with high fan-out. It represents the main part of the NAL and is equal to

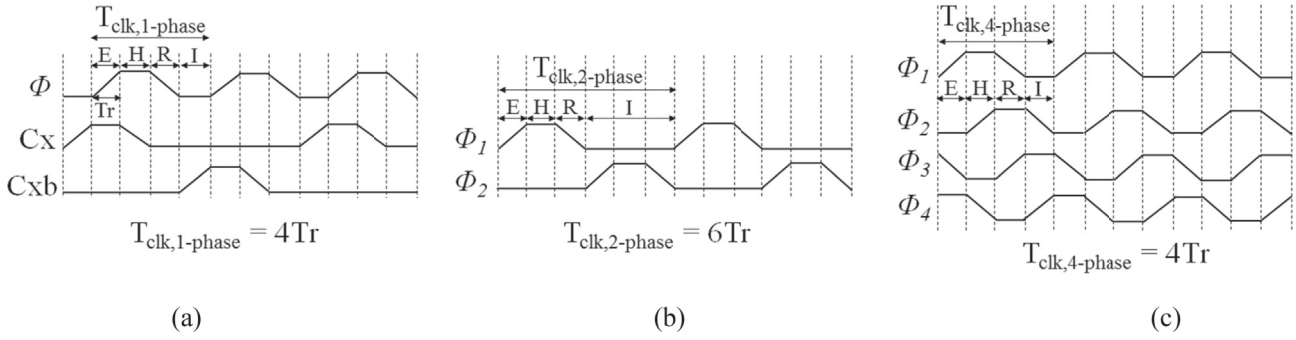

Fig. 2. Power-clocking scheme (a) single-phase (b) 2-phase (c) 4-phase.

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