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# Examining epitaxial graphene surface conductivity and quantum Hall device stability with Parylene passivation

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## ARTICLE INFO

## ABSTRACT

Homogeneous, single-crystal, monolayer epitaxial graphene (EG) is the one of most promising candidates for the advancement of quantized Hall resistance (QHR) standards. A remaining challenge for the electrical characterization of EG-based quantum Hall devices as a useful tool for metrology is that they are electrically unstable when exposed to air due to the adsorption of and interaction with atmospheric molecular dopants. The resulting changes in the charge carrier density become apparent by variations in the surface conductivity, the charge carrier mobility, and may result in a transition from n-type to p-type conductivity. This work evaluates the use of Parylene C and Parylene N as passivation layers for EG. Electronic transport of EG quantum Hall devices and non-contact microwave perturbation measurements of millimeter-sized areas of EG are both performed on bare and Parylene coated samples to test the efficacy of the passivation layers. The reported results, showing a significant improvement in passivation due to Parylene deposition, suggest a method for the mass production of millimeter-scale graphene devices with stable electrical properties.

## 1. Introduction

Over the last few years, graphene has become a beacon to many scientific communities, partially because of its useful electrical properties [1–3]. Graphene can be grown on silicon carbide (SiC) substrate by silicon sublimation, and it has been demonstrated that this form of graphene exhibits properties that make it appropriate for use in metrological applications like developing a quantized Hall resistance (QHR) standard [4–10]. Developing this standard would require the properties of millimeter-scale EG devices, such as the surface conductivity, carrier density, and mobility to be relatively stable over time and unaffected by changes in the environment. Although millimeter-scale EG devices have already been realized for metrology, passivation efforts for devices of this size and application have not been heavily explored [11,12]. Similar work has been reported for much smaller EG devices, but quantum Hall measurements were not monitored [13].

If left exposed to air at ambient atmospheric conditions, the carrier density and surface conductivity of the unprotected EG varies over time

[14–17]. Because electrical stability is vital to the mass production of EG for other large-scale electrical applications, finding a suitable passivation material is a high priority. This holds especially true in the field of electrical metrology, where desired passivation entails electrical properties to be stable within unit percentages over several weeks in air. Efforts have been made to understand multiple forms of epitaxial graphene passivation, with some forms involving the use of poly-methyl methacrylate (PMMA) [18], various dielectric materials available with atomic layer deposition tools [19–22], and amorphous boron nitride [13,23]. One of the main issues with atomic layer deposition is the imparted carrier density by the various films, which span from $5 \times 10^{12}\, cm^{-2}$ to $9 \times 10^{12}\, cm^{-2}$. For resistance metrology, densities on order of $10^{12}$ or lower are required for epitaxial graphene devices to outperform the current standards based on gallium arsenide.

One possibility for passivation popular with organic field effect transistors and similar devices is Parylene, which shows excellent promise for stabilizing mass-producible electronics [24–29]. In this work, we report on the use of Parylene C and Parylene N as

encapsulating agents for EG. Their effectiveness to protect both EG quantum Hall devices and large areas of unprocessed monolayer EG is evaluated by remeasuring the electrical properties of samples after they have been exposed to various environmental conditions, such as a high temperature or high humidity. We report that Parylene C and N can passivate the surface conductivity to within 20% of its previously measured value for EG areas on millimeter scales, and these results, despite not meeting the criterion for electrical resistance metrology, may have a more fruitful impact on general device engineering that does not rely on measuring resistances to one part in 10 [8]. A general, added advantage to using Parylene is that devices can be fully packaged and wire-bonded before deposition, enabling testing before process steps.

## 2. Sample preparation

### 2.1. High temperature EG growth

EG is formed by sublimating Si atoms from the surface of the SiC substrate's Si face during an annealing process. Samples used for this study were grown both on square and rectangular SiC chips diced from 76 mm 4H-SiC(0001) semi-insulating wafers (CREE[see notes]) which has a miscut of about 0.10°. SiC chips were then submerged in a 5:1 diluted solution of hydrofluoric acid and deionized water, making an effective concentration of < 10%. Following a deionized water bath, chips were placed on top of a polished pyrolytic graphite substrate (SPI Glas 22[see notes]) with the SiC(0001) face resting against the graphite. The gap between the two surfaces creates a diffusion barrier for escaping Si atoms which promotes homogeneous graphene growth conditions [6]. Some of the graphene samples were prepared with polymer-assisted sublimation growth [30]. The annealing process was performed in ambient argon with a graphite-lined resistive-element furnace (Materials Research Furnaces Inc.[see notes]), with heating and cooling rates of about 1.5 °C/s. The growth chamber was evacuated and flushed with 100 kPa Ar from a 99.999% liquid Ar source, and the growth stage was performed at 1900 °C [12]. After growth, EG was checked with confocal laser scanning and optical microscopy to allow for quick identification of successful growth over large areas [31].

### 2.2. Device fabrication and large area EG preparation

For electronic transport measurements, quantum Hall devices were fabricated in the same fashion as in previous works [12,13]. In summary, a protecting layer of Au was placed on the chip prior to the multiple lithography steps required to etch out the Hall bar and its contact pads. Devices were fabricated on the smaller square chips measuring 7.6 mm by 7.6 mm while EG samples for microwave cavity perturbation measurements were etched into a well-defined rectangular shape, measuring 4.04 mm by 10 mm, on a chip whose dimensions were 15.2 mm by 7.6 mm. The shape of the EG area, which will be described in more detail later, was important for analyzing data from the microwave cavity measurements.

### 2.3. Parylene deposition

For graphene encapsulation, two species of poly[para-xylylene], commonly known as Parylene C and Parylene N, were used in different sets of experiments and obtained from Specialty Coating Systems[see notes]. To deposit a layer with a thickness of 720 nm, a sub-gram amount of di-para-xylylene dimer was weighed and placed in an aluminum boat. For Parylene C and N, the contents of the boat were vaporized at 175 °C and 160 °C, respectively. The Parylene C and N was pyrolyzed at 690 °C and 650 °C to break the dimer and the resulting monomer para-xylylene was applied to the sample as a gas. The film was formed over a duration of about 6 h by polymerization of the gaseous compounds on the cooled sample surface at 25 °C.
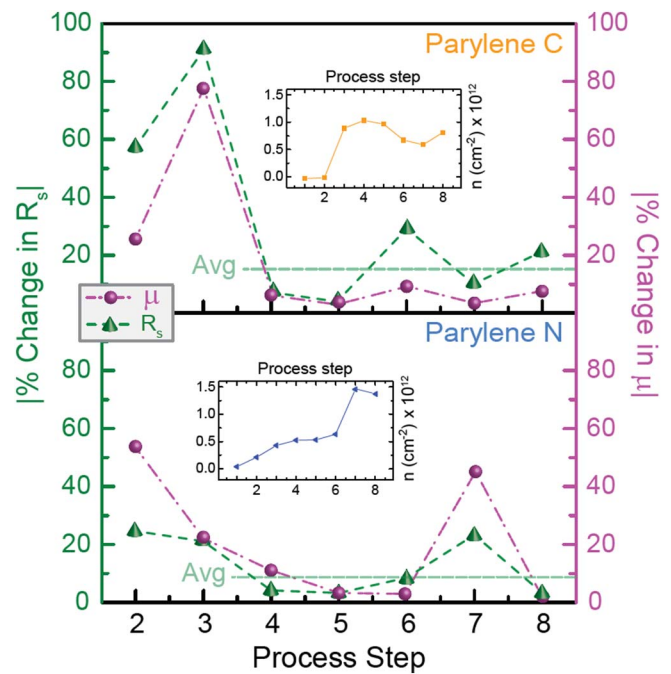


**Fig. 1.** The sheet resistance (green data points and axis) and mobility (purple data points and axis) are shown as a percentage change from their previous values after each process step. The insets show the example device's carrier density measured as a function each step. The average modulations of the sheet resistance are shown as transparent, horizontal, green lines and represent the data after stabilization around process step 3. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

## 3. Characterization and experimental techniques

### 3.1. Device transport measurements

Transport measurements of our EG devices were performed at 1.6 K in a 9 T superconducting magnet cryostat. Once the devices were fabricated, they were characterized by atomic force microscopy and Raman spectroscopy [32], and were mounted onto sample holders for magneto-transport measurements. The measurements were collected using a Labview[see notes] script to acquire *I–V* curves, magnetic field sweeps, and temperature data. The three main device characteristics of interest were longitudinal resistance ($R_{xx}$, or alternatively represented as *sheet resistance* $R_s = R_{xx}\frac{W}{L}$), device mobility ($\mu$), and carrier density ($n_e$). By measuring the Hall resistance ($R_{xy}$) as a function of the magnetic field, one can extract the carrier density by recalling the simple formula: $n_e = \frac{1}{e\left(\frac{dR_{xy}}{dB}\right)}$. Furthermore, the mobility is linked to both the carrier density and the sheet resistance via: $\mu = \frac{1}{en_eR_s}$. In these formulas, $e$ is the electron charge, $W$ and $L$ are the respective width and length of the Hall bar, and the derivative is approximated from a best-fit line of the $R_{xy}$ voltages measured while sweeping the B-field through low values (< 1 T).

### 3.2. Environmental exposure conditions

After the sample was initially characterized, a series of various controlled environmental conditions were imposed on the samples, which included changes in both temperature and relative humidity. We used a Thermotron[see notes] testing chamber for these exposures since the chamber was able to maintain, for any given exposure, a stable temperature and humidity (within 0.1% of the parameter value).