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Fast breaker failure backup protection for HVDC grids☆

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ABSTRACT

High voltage direct current (HVDC) grid protection must clear dc faults within a time-frame of milliseconds to avoid damages to power electronic components due to fast rising dc fault currents. If the breaker associated with the primary protection fails, backup must be provided to clear the faults which would otherwise persist. Backup relaying algorithms originally developed for ac systems delay the detection of primary protection failure until the expected primary fault clearance instant. Application of similar algorithms to HVDC grids results in a long fault clearing time, which requires converters and breakers to withstand unrealistically large currents. To reduce the fault clearing time, this paper proposes two fast backup relaying algorithms which detect local and remote breaker failure before the expected primary fault clearance instant. The proposed algorithms use thresholds on the voltage and current measurements to detect breaker failure. They are evaluated using a four-terminal HVDC grid test system implemented in PSCAD. The study results show that the proposed algorithms can reliably detect breaker failure within few milliseconds after fault inception. Furthermore, the algorithms provide faster backup protection compared to methods based on ac backup protection philosophy. The resulting decreased fault clearance time reduces the maximum dc fault current and consequently, leads to lower required ratings for HVDC grid equipment.

1. Introduction

Voltage source converter (VSC) high voltage direct current (HVDC) systems are expected to play an important part in the future European electricity system [1]. Beside point-to-point connections, VSC HVDC grids are considered to efficiently integrate renewable energy sources and to facilitate a pan-European energy market. An essential feature of a reliable HVDC grid is protection against short-circuit faults on dc lines or buses. The main challenge for HVDC grid protection is the required high operation speed, as dc fault currents quickly increase to high steady-state values [2]. These currents should be interrupted fast enough to avoid damages to the power electronic components. HVDC grid protection must operate one order of magnitude faster than its ac counterpart [3].

Various algorithms have been proposed for fast and selective HVDC grid primary protection [4–7]. These algorithms detect the fault and identify its location within a few milliseconds. To confine the fault impact to the faulted line, a selective fault clearing strategy clears the fault by opening the dc breakers at the two ends of the faulted line [8]. By contrast, non-selective fault clearing strategies interrupt dc fault currents through combined action of multiple equipments such as converters with fault blocking or fault current limiting capability [9–13]. For non-selective strategies, dc faults typically affect the entire or a large section of the HVDC grid. As non-selective methods are only effective in small systems, this paper focuses on selective fault clearing algorithms.

For selective HVDC grid protection, backup protection is required in case of primary protection failure. A primary protection failure can be caused by a malfunction of the primary relay, breaker or communication system [14]. In ac systems, the backup protection operation is delayed with respect to the primary protection to allow the latter to initially deal with the fault [15].

A relaying algorithm for backup protection in HVDC grids is proposed in [4]. This algorithm detects primary protection failure if the current through the primary breaker does not become zero at the expected primary clearing instant. The disadvantage of this algorithm is its long fault clearance time [16]. In [17], breaker internal measurements are used to determine primary breaker failure. Although this algorithm is fast, its dependence on internal measurements of the breaker limits its application in multi-vendor HVDC grids.

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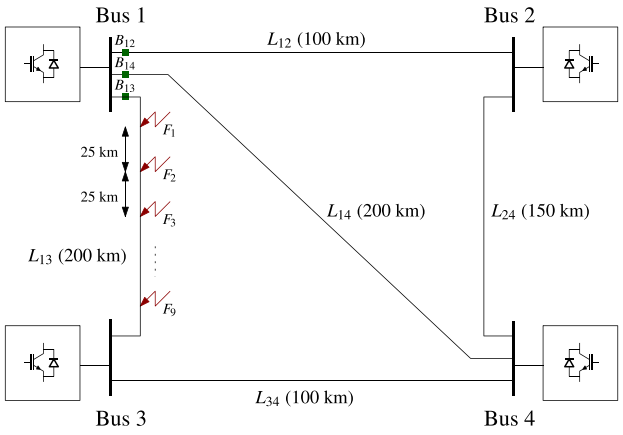

Fig. 1. Four-terminal HVDC grid test system.

This paper proposes two fast relaying algorithms for local and remote breaker failure backup protection. The proposed breaker failure backup relaying algorithms distinguish cleared faults from uncleared ones during the fault clearing process of primary protection. Since these algorithms only use primary voltage and current measurements at line ends, their performance is independent of breaker internal characteristics.

The paper is structured as follows: Section 2 presents the HVDC grid test system and its components' models. This section also provides an analysis of the voltage and current waveforms in the test system after a fault. Section 3 presents the principles of breaker failure backup relaying algorithms. The application of the proposed relaying algorithms to an HVDC grid test system is presented in Section 5. Conclusions are stated in Section 6.

2. HVDC grid model and dc fault analysis

2.1. HVDC grid model

The four-terminal HVDC grid test system of [18] was used for the studies of this paper (Fig. 1). In this test system, four half-bridge modular multilevel converters are connected via five cables to form a meshed HVDC grid. A dc breaker is included at the end of each cable. An inductor that limits the rate of rise of the fault current is located in series with each dc breaker. The system parameters and components' models are similar to those of [18], except for the series inductor value which has been reduced to 50 mH. This section briefly presents the model of cables, converters and breakers considered in the transient simulation studies. The simulations were performed in PSCAD.

2.1.1. Cable model

To accurately simulate the high frequency transient waveforms after a dc fault, the cables are represented by the frequency dependent (phasor) cable model. This is a distributed parameter model which takes the frequency dependency of cable parameters into account [19]. The cable used in the studies of this paper has a surge impedance of 33.7 Ω and a traveling wave speed of 183.46 km/ms (evaluated at a frequency of 1 MHz).

2.1.2. Converter model

The converters are represented by a continuous model with blocking capability to speed up simulations while providing adequate accuracy [20]. In this model, instead of modeling all individual submodules, each converter arm is represented with a continuous voltage source. The converter's insulated gate bipolar transistors (IGBTs) are blocked if the arm current exceeds 1.6 times the IGBT continuous current. This protects the IGBTs against overcurrents since the maximum instantaneous overcurrent that an IGBT can safely tolerate is around two times its continuous current.

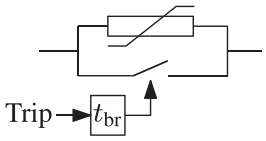

Fig. 2. Hybrid HVDC breaker model.

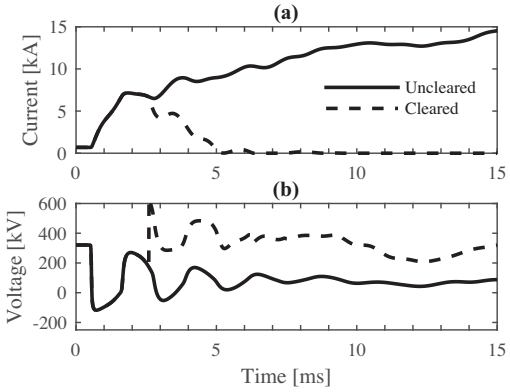

Fig. 3. Voltage and current at R_{13} for a fault in the middle of L_{13} (solid: uncleared due to breaker B_{13} failure, dashed: cleared by primary protection).

2.1.3. Breaker model

Hybrid dc breakers are considered for the studies of this paper. The hybrid breaker is modeled as a switch in parallel with a surge arrester (Fig. 2). After a certain time delay t_{br} from the instant the breaker receives a trip signal, it inserts a countervoltage in the system. The value of the countervoltage is determined by the rating of the parallel surge arrester and is typically 1.5 times the rated dc voltage (480 kV in this case). The time delay t_{br} represents the time required by the dc breaker to open after receiving the trip signal and is assumed to be 2 ms for the considered dc breakers [8].

2.2. Fault analysis

As an example, the waveforms seen by relays R_{13} and R_{31} for a solid pole-to-pole fault in the middle of line L_{13} and a similar fault at bus 1, are analyzed. The waveforms are obtained by voltage and current measurements at the cable side of the breaker inductor. For both faults, two scenarios in which breaker B_{13} clears the fault or fails in removing the fault, are discussed.

2.2.1. Pole-to-pole fault at L_{13}

After fault inception, the voltage and currents measured at R_{13} show the successive reflections of the fault wave between the fault location and breaker series inductor (Fig. 3, solid line). The fault occurs at $t = 0$ ms and creates a traveling wave which arrives at the two terminals of L_{13} at $t = 0.54$ ms due to the finite traveling wave speed. The fault wave travels back and forth between the two discontinuities on L_{13}, i.e., series inductor and the fault location, and results in successive reflections at the terminals. In the literature, several algorithms are proposed for detecting and identifying faults based on these reflections [6,7,21].

The voltage and current waveforms for the two scenarios differ after $t = 2.54$ ms, which is equal to the sum of the time required for the wave to travel from the fault location to R_{13}, the fault detection time and breaker opening time (Fig. 3). If B_{13} fails to clear the fault, the voltage measured at the end of the faulted line decreases to a