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Performance assessment of distance protection fed by capacitor voltage transformer with electronic ferro-resonance suppression circuit

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ABSTRACT

Distance relay may over-reach when the voltage information is delivered from capacitor voltage transformer (CVT) and when source to line reach impedance (SIR) is high. A technique adopted recently involves attacking the CVT transient problem from source side itself, i.e., by using electronic ferro-resonance suppression circuit (FSC), rather than allowing the transients and tackling this issue in the relay by providing adaptive zone 1 reach, providing a fixed time delay or using a narrow band pass filter which increases the total fault clearing time by the local relay. The work in this paper investigates the performance of CVT with electronic FSC for different fault, loading and SIR conditions.

1. Introduction

Capacitor voltage transformers are typically used in switch yards for economic reasons to deliver primary voltage information to protective relays and metering units. The current information is fed from current transformer (CT). These instrument transformers, CVT and CT, deliver the fault information to protective relays. The performance of the protective relay depends directly on the fault information delivered by the instrument transformers. Distance relay estimates the positive sequence impedance by extracting the fundamental frequency information from voltage and current signals. The extracted samples are usually pre-processed by digital filters to improve distance relay performance, e.g., digital mimic filter or double differentiator (DD) is typically used in the current signal path to remove dc offset to prevent distance relay to over-reach. Even though the samples are pre-processed before transforming the time domain information to frequency domain information, the distance relay may mal-operate due to many reasons like CVT transients [1], power swings, severe loading conditions, the presence of series capacitor, etc. In order to handle this, additional logics are used to supervise the trip decision. Solutions like blinder schemes, load encroachment function and using memory for polarizing signals are currently available in an intelligent electronic device (IED).

Table 1
Techniques used in IEDs to handle CVT transients.

Manufacturer	Technique
SIEMENS [4]	Adaptive algorithm to reduce zone 1 reach
GE [2]	Use of double zone 1, inner zone 1 reach is dynamic without delay, whereas outer zone 1 has time delay
SEL [5]	Patented technique to block trip signal based on frequency domain information, if high SIR is detected
ABB [6], GE [7], AREVA [8]	Special filters are introduced in voltage path if high SIR is detected

CVT transients during high SIR conditions cause the distance relay to over-reach, as the transients may be close to the fundamental frequency. As SIR is inversely proportional to voltage at fault point [2], high SIR results in low fault voltage. This results in low signal to noise ratio which introduces error in phasor estimation as distance relay uses either full cycle or half cycle discrete Fourier transform (DFT). Table 1 shows the techniques available in today's intelligent electronic devices to prevent distance relay mal-operation caused by CVT transients during high SIR condition, which is defined [3] in Eq. (1),

$$\text{SIR} = \frac{\text{source impedance behind relay terminal}}{\text{line impedance}} \quad (1)$$

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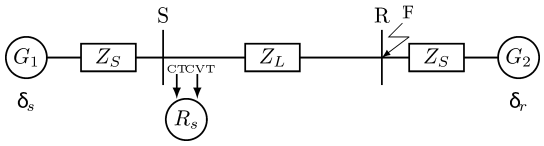

Fig. 1. Test system under consideration.

Although the solutions provided in today's IED may prevent relay mal-operation caused by CVT transients, this is achieved by scarifying tripping time delay. Many solutions are proposed [9–14] to overcome distance relay mal-operation, but the proposed solutions are not focused to damp the oscillations in voltage signal delivered by CVT. Other group of researchers [15,16] attacked this issue from the source side itself, i.e., by replacing the existing active (A)/passive (P) FSC with electronic (E) FSC, but the performance of the electronic FSC in terms of reach has not yet been analyzed. In order to fill this gap, investigation is carried out by using frequency dependent [17] transmission line model (Z_L) for a 200 km long transmission line [18], distributed parameter model for source impedance (Z_S) (Appendix C), CVT (Appendices A and B), CT (Appendix E) model, bus bar model (Appendix D) and primary arc model [19] in Alternative Transient Program (ATP).

2. Test system and results

Fig. 1 shows the test system under consideration where single phase to ground faults (SPGF), phase to phase and ground faults (PPGF) and 3 phase to ground fault (3PGF) are applied on the receiving end bus. Fig. 2 shows the detailed model of CVT considered for analysis. Fig. 3 shows the FSC models used in Fig. 2. The control part in electronic FSC is achieved using MODELS, a general-purpose description language in ATP using FORTRAN. The performance of IED (R_s) fed by CVT with active, passive and electronic FSC at the sending end is monitored for different loading

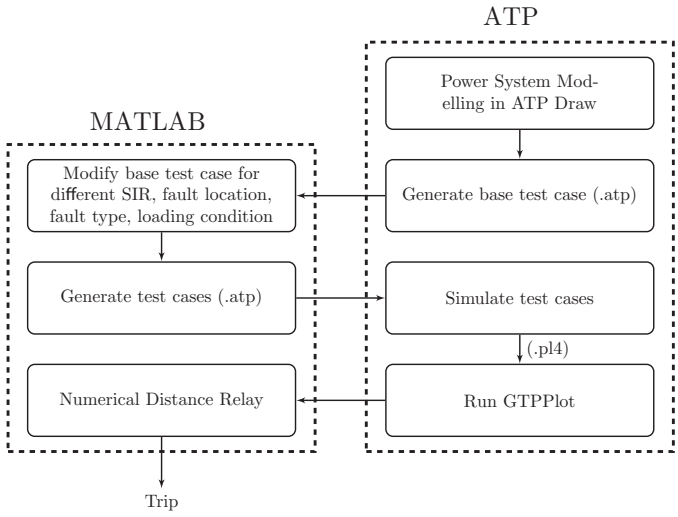

Fig. 4. Batch mode simulation using ATP and MATLAB.

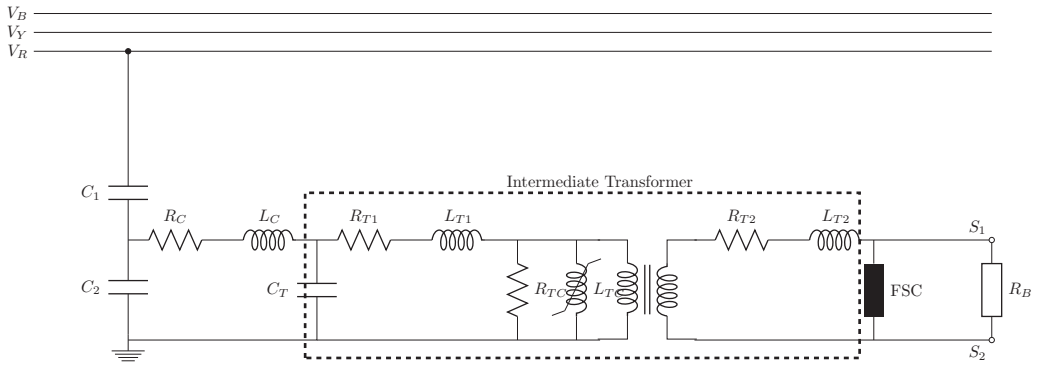

Fig. 2. Detailed model of CVT.

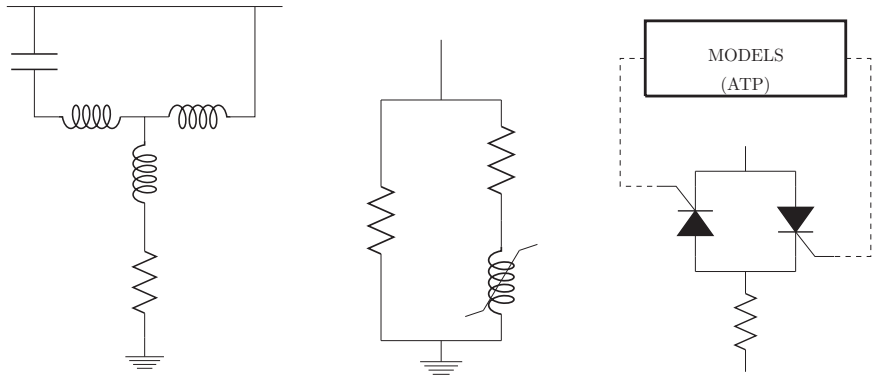

Fig. 3. FSC types.