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Constant power load stabilization

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ABSTRACT

Stabilization of constant power loads (CPLs) fed through poorly damped input LC filters involves a trade-off between well damped filter quantities and small generated power modifications, where power modifications in general may be generated by internal CPL power control or by additional hardware. To simplify this trade-off, an explicit controller expression is presented, directly parameterized in terms of a damping factor. By also deriving damping factors corresponding to stabilization with minimal power modifications, tuning of stabilization becomes straight forward. Although applicable to most stabilization schemes, realization of the proposed stabilization is illustrated with an induction motor drive, using hardware-in-the-loop simulations.

1. Introduction

Electric power systems, appearing in an increasing number of applications, typically use switched power converters to control the flow of power. To suppress high frequency switching harmonics, but also to provide stable input quantities, hardware input filters are often added to the converters. However, with tight power control of the converters, it is well-known that these filters may generate stability problems. This follows since converters efficiently suppressing the effect of input voltage variations approximately act as constant power loads (CPLs). The converters therefore represent incremental negative resistances to the input filters and since these often are poorly damped to minimize power losses, the system may become unstable, see e.g. Singh et al. (2017) and Wu and Lu (2014) for an overview. To solve such stability problems (with a general CPL), the interaction between the input filter and the CPL must be modified. This may be achieved by adding extra filter components as proposed in Cespedes et al. (2011), Dzhankhotov and Pyrhonen (2013) and Erickson (1999), or by inserting additional dc/dc controlled converter storage systems, see Inoue et al. (2012), Carmeli et al. (2012) and Kim et al. (2016). An alternative to adding hardware components is to instead modify the power consumed by the CPLs themselves, see e.g. Glover and Sudhoff (1998), Jänecke (1992), Lee and Sul (2014), Liu and Forsyth (2008), Liu et al. (2007), Mohamed et al. (2012), Mosskull et al. (2007) and Walczyna, Hasse, and Czarnecki (1996). The obvious advantage with the latter methods is that they do not increase complexity, cost, size and power losses of the system. However, the introduced disturbances of the CPL power may instead interfere with internal control objectives by limiting achievable power control bandwidth and requiring increased control margins.

In the literature, focus of stabilization design is often limited to assuring system stability. However, in practice, this may not be enough, but also a certain damping of filter quantities is desired. Sudden changes in the supply voltage should e.g. not result in under- or overvoltages, causing system shutdown. On the other hand, well damped filter quantities typically require larger modifications of the original system, which increase size and power losses of additional hardware components, or represent larger disturbances to the CPL power control. To uniformly quantify such undesired effects, the different stabilization schemes are here represented by the corresponding generated power modifications. Independently of how stabilization is realized, stabilization design may then be formulated as finding the best trade-off between damping of filter quantities and the size of the required power modifications (subject to stabilizing the system). This should further hold at all relevant operating points. Once a desired power modification has been derived, it can be directly applied with any active stabilization method (only considering the specific power control dynamics), but can also be used as guiding lines for passive filter design. To formalize the stabilization problem, the two conflicting design goals described above are summarized in Table 1, where also a robustness requirement to model errors has been added. In the table, the first two goals will be referred to as performance requirements and the third to as a robustness requirement.

Normally, all the design goals in Table 1 are not simultaneously addressed during stabilization design. For example, for the special case of input LC filters, only damping is directly considered in Liu et al. (2008), whereas power modifications are analytically minimized in Mosskull (2014, 2015a), without explicitly considering damping

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Table 1
Stabilization design goals.

1. Small power modifications due to stabilization
2. Well damped system dynamics
3. Robustness to model errors

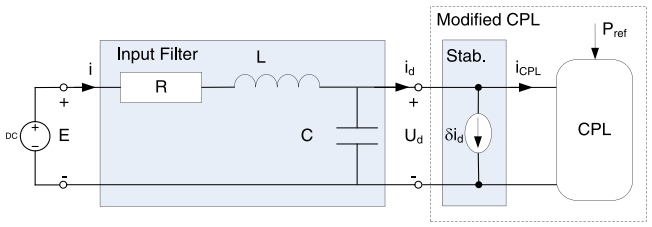

Fig. 1. Constant power load (CPL) fed through an input filter. Stabilization has also been added in the general form of a current source modifying the output current (or power) of the input filter.

requirements. On the other hand, with the model predictive control (MPC) approach to stabilization chosen in Smidl et al. (2015), the trade-off might be handled through weight parameters for different filter quantities included in a quadratic cost function. It is, however, not clear how these design parameters should be chosen or updated with the operating point. To improve stabilization design, explicitly considering the trade-off between good damping and small power disturbances, stabilization is here parameterized in terms of a damping factor. It is shown that stabilization for minimal power modifications as derived in Mosskull (2014, 2015a) also can be represented this way, where the corresponding damping factors naturally represent boundary values for stabilization design.

The design goals of Table 1 are expressed mathematically in Section 2 for general CPLs fed through general input filters. Stabilization is also formally posed as an optimization problem, aiming at minimizing power modifications subject to meeting the damping and robustness constraints. For the important special case of input LC filters, it is shown in Section 3 how the trade-off between the two performance goals in Table 1 can be handled by explicitly expressing stabilization in terms of a damping factor of the filter quantities, with the minimal power modifications derived in Mosskull (2014, 2015a) as special cases. Actual realization of the derived stabilization structure is demonstrated with an induction motor (IM) drive using hardware-in-the-loop (HIL) simulations in Section 4. Conclusions are finally given in Section 5.

2. CPL stabilization

Based on the results of Mosskull (2014, 2015a, 2015b), this section presents a framework for analysis and design of stabilization of general CPLs fed through input filters as shown in Fig. 1. Although an LC filter is explicitly depicted, which is an important special case, the analysis in this section is valid for general input filters. In the figure, stabilization is further represented as an additional current source modifying the current flowing out of the input filter. The current source may represent passive stabilization, where the additional current component $\delta i_d(t)$ (producing a power modification $\delta P(t)$) is generated by connecting extra filter components at the filter output terminals as proposed in Cespedes et al. (2011), Dzhankhotov and Pyrhonen (2013) and Erickson (1999). It may also represent active stabilization, where the current component is either consumed by auxiliary systems added between the filter and the CPL (Carmeli et al., 2012; Inoue et al., 2012; Kim et al., 2016), or by the CPL itself (Glover & Sudhoff, 1998; Jänecke, 1992; Lee & Sul, 2014; Liu et al., 2007; Liu & Forsyth, 2008; Mohamed et al., 2012; Mosskull et al., 2007; Walczyna et al., 1996).

The design goals in Table 1 are mathematically expressed in terms of closed-loop transfer functions in Sections 2.1–2.3. System excitation is considered both through the supply voltage $E(t)$ and the consumed CPL power denoted $P_{CPL}(t)$. The two excitation signals lead to two different and possibly coupled stabilization problems, here referred to as *disturbance rejection* and *reference tracking*, respectively. It is further shown that the two performance goals in Table 1 are coupled, whereas robustness can be separately optimized if the two excitation signals and some internal filter quantity are available to stabilization. Otherwise, also the performance and robustness goals are coupled. The mathematical representation is then used to derive a new very general result on performance limitation in Section 2.4. Stabilization is finally posed as an optimization problem in Section 2.5, aiming at minimizing power (current) modifications subject to meeting the damping and robustness requirements.

Note that the consumed CPL power $P_{CPL}(t)$ in some applications can be considered generated from a power reference $P_{ref}(t)$, see Fig. 1. In these cases, the nominal CPL power may be represented as $P_{CPL}(t) = G_c P_{ref}(t)$, where the transfer function G_c models the closed-loop power dynamics of the CPL.

2.1. Linear system model

A general reciprocal input filter can be represented as a two-port with inverse hybrid parameters as

$$\begin{pmatrix} i(t) \\ U_d(t) \end{pmatrix} = \begin{pmatrix} Y_{in}(p) & -G_E(p) \\ G_E(p) & Z_{DC}(p) \end{pmatrix} \begin{pmatrix} E(t) \\ -i_d(t) \end{pmatrix}, \tag{1}$$

where p represents the derivative operator and Y_{in}, G_E and Z_{DC} are linear transfer functions. Moreover, $E(t)$ and $i(t)$ in Eq. (1) represent the supply voltage and input current, whereas $U_d(t)$ and $i_d(t)$ are the dc-link voltage and current, respectively. Note the direction of $i_d(t)$ in Fig. 1, which explains the minus sign of $i_d(t)$ in Eq. (1).

The dc-link current $i_d(t)$ can further be expressed as the consumed power $P(t)$ divided by the dc-link voltage $U_d(t)$. Linearizing this equation results in

$$i_d(t) = \underbrace{\left(-\frac{P_0}{U_{d0}^2}\right)}_{\triangleq Y_{DC0}} U_d(t) + \frac{1}{U_{d0}} P(t), \tag{2}$$

where P_0 and U_{d0} represent steady-state values (and the signals actually describe deviations from the stationary operating point although not explicitly reflected in the notation). Eq. (2) also defines the admittance Y_{DC0} for a (perfect) CPL, which follows from the equation, since the power $P(t)$ (by definition) is independent of the dc-link voltage. At positive power, the admittance Y_{DC0} in (2) is negative and therefore reduces damping. The destabilizing effect increases with power and the system may eventually become unstable. The maximum power assuring stability can be estimated through the Middelbrook stability criterion, which states that the system in Fig. 1 is stable if $\|L_{DC}\|_\infty < 1$ (Middlebrook, 1976). By using the admittance expression for Y_{DC0} in Eq. (2), this (sufficient) stability condition can be rewritten in terms of the consumed load power as $|P_0| < U_{d0}^2/\|Z_{DC}\|_\infty$. Hence, with large resonance peaks of the filter transfer function Z_{DC} (poor damping), the power limit for stability may be very low and the system hence not practically usable.

To stabilize the system, an additional input admittance term δY_{DC} of the CPL can be emulated by varying the additional current component $\delta i_d(t)$ in Fig. 1 as a function of the dc-link voltage. From Eq. (2), this additional current component can also be represented as an additional power component $\delta P(t) = U_{d0}\delta i_d(t)$. The total power $P(t)$ consumed by the modified CPL in Fig. 1 is then represented as

$$P(t) = \underbrace{G_c P_{ref}(t)}_{P_{CPL}(t)} + \delta P(t), \tag{3}$$

where $P_{CPL}(t)$ hence represents the nominal CPL power (without stabilization).