Materials Science in Semiconductor Processing 30 (2015) 18–24

Contents lists available at ScienceDirect

Materials Science in Semiconductor Processing

journal homepage: www.elsevier.com/locate/mssp

Study on post-deposition annealing influenced contribution of hole and electron trapping to threshold voltage stability in organic field effect transistors

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ARTICLE INFO

Available online 31 October 2014

Keywords:
OFET
Copper phthalocyanine
Annealing
Threshold voltage stability

ABSTRACT

The effect of post-deposition annealing of copper phthalocyaine (CuPc) film acting as active layer, on the hysteresis and the threshold voltage stability of organic field effect transistors (OFETs) was studied. The morphology of annealed CuPc film, as verified by Atomic Force Microscopy (AFM), showed well connected grains, but also increase in surface roughness which could be due to desorption of certain number of CuPc molecules causing voids. Increase in hysteresis in the transfer characteristics and the threshold voltage shift were observed for devices with annealed films as compared to that for devices with as deposited films. Presence of both hole and electron trapping effects causing hysteresis were observed where hole trapping was found to be the dominant cause for hysteresis and threshold voltage shift in devices with annealed films. This could be attributed to increase in grain boundary density in CuPc films with annealing. Electron trapping effect was explained to be influenced by both increased silanol groups on dielectric surface caused by diffusion of oxygen and moisture from ambient through voids as well as by hole trapping effect itself.

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1. Introduction

Recently organic field effect transistors (OFET) have attracted much attention due to their potential use in a variety of large area electronic applications such as displays, sensors, electronic bar codes etc. Of the many organic semiconducting materials, small molecules such as copper phthalocyanine, pentacene etc. that can be deposited in thin film form with a high degree of molecular ordering show the best performance. Most of these materials are thermally evaporated and the resulting film is polycrystalline in nature. Since OFETs are generally working in accumulation regime and most of the modulated charge lies close to the semiconductor/dielectric interface within the first few nm, the molecular ordering of the active layer at the interface is crucial for improvement in mobility as well as threshold voltage instability. Several techniques that have been employed to improve the ordering of these films are 1) varying the deposition parameters of semiconducting materials, like substrate temperature, deposition rate [1], 2) post-deposition annealing of active materials [2], 3) suitable treatment of the inorganic dielectric with self assembled monolayers (SAM) [3] or polymer films [4]. Though there are several reports on the effect of dielectric modification, the effect of post-deposition annealing on the performance of OFETs has been scarcely studied and show widely varying results.

Hysteresis observed in transfer characteristics during repeated cycles of operation of OFETs, especially when SiO_2 dielectric is used results in such threshold voltage instability. Hysteresis found in devices with SiO_2 dielectric

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http://dx.doi.org/10.1016/j.mssp.2014.09.038
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are mostly attributed to charge traps in bulk SiO_2, oxygen or moisture related defect trap sites in the semiconductor and/or mobile ions in the dielectric. Hysteresis can either be in clockwise or anticlockwise direction depending on the root cause of hysteresis. If polarization or mobile ions in dielectric cause hysteresis, it is known to be in clockwise direction while traps at semiconductor itself mostly cause anticlockwise hysteresis [5]. Many studies show that modifying the dielectric with suitable polymer layer minimizes the number of hydroxyl groups at the interface thus reducing the trap sites and hysteresis [4]. Post-deposition annealing of semiconducting films is also shown to result in lesser instability after encapsulation of films under inert atmosphere [2] while some reports mention the return of hysteresis in OFETs when exposed to atmosphere [6]. Since only very few reports are available on the effect of post-deposition annealing on threshold voltage stability, more studies are required in this direction. As post-deposition annealing is commonly used to improve mobility, it is very essential to determine if this increased mobility is occurring at the cost of threshold voltage instability. In this work we have used copper phthalocyanine (CuPc) as the active material since CuPc is a chemically and thermally stable *p*-type material that can be obtained commercially in high purity. SiO_2 is used as the inorganic dielectric due to its well studied dielectric properties in Si based FETs. Though we observed significant improvement in mobility with post-deposition annealing [7] in our previous study, we did not discuss hysteresis effect, which is discussed in detail in this study. Many of the studies discussing hysteresis generally attribute it to either hole trapping or electron trapping [8,9]. In our previous studies on OFETs with as deposited CuPc films, we have observed that both holes and electrons contribute to hysteresis and threshold voltage shift [10]. The dominance of holes or electrons is being influenced by the growth conditions of CuPc films, like substrate temperature, nature of dielectric, post-deposition annealing, active layer thickness etc. We have concluded in that study that hole trapping is mainly decided by grain boundary density, while electron trapping predominantly occurs at dielectric/semiconductor interface though it can partly occur at the grain boundaries also. It is well discussed in the literature that oxygen or moisture from ambient diffusing into the interface aggravates charge trapping [11,12]. Since the present study is carried out in air and there is change in morphology and grain boundary density with annealing, apart from studying threshold voltage instability, it is also essential to determine how hole and electron traps get influenced by the above mentioned factors after annealing. To our knowledge, there are no studies in the literature which discuss how hole or electron traps get modified with post-deposition annealing.

2. Experimental details

For top contact OFET device structure used in this work, highly doped *n* type (100) silicon wafer (0.01–0.015 Ω cm) was used as substrate and gate electrode, with 200 nm thermally grown SiO_2 layer acting as the gate dielectric. The substrate was ultrasonically cleaned using trichloroethylene, acetone and methanol and dried with nitrogen gas. Copper phthalocyanine (CuPc), purchased from Sigma-Aldrich and used as received, was thermally evaporated above the SiO_2 layer at a pressure of 1×10^{-5} mbar. The evaporation rate was maintained at 0.5–1 Å/s and the thickness of the film was about 30 nm, as measured by quartz crystal thickness monitor. The substrates were maintained at room temperature during the deposition of CuPc (device1). The OFET device was fabricated by thermally evaporating gold through a shadow mask for source (*S*) and drain (*D*) electrodes above CuPc film with channel length and width of 25 μm and 2 mm, respectively. For studying the effect of post deposition annealing, CuPc films on SiO_2 were annealed at 170 (device 2) and 225 °C (device 3) for 4 h before depositing source and drain electrodes. For capacitance measurements, gold electrodes of area 25×10^{-4} cm^2 were deposited through a shadow mask on the gate dielectrics to form the Au/dielectric/Si(p^+) (MIM) structure and the measurements were carried out using Agilent 4284 A LCR meter. The current–voltage (*I*–*V*) characteristics were measured using Keithley voltage source current meter, (model 6487) in air at room temperature. Structure of the films was determined by X-ray diffraction measurements using RIGAKU analytical X-ray diffraction system (Model: RINT 2000 Dmax) carried out using Cu Kα radiation. Surface morphology of CuPc films was verified using Atomic Force Microscope (AFM) (NT MDT SOLVER P47).

3. Results and discussion

3.1. Structural characterization

Surface morphologies of as deposited and annealed (at 170 °C, 225 °C) CuPc films are shown in Fig. 1 along with their corresponding roughness profiles. Coagulation of grains appear to be occurring after annealing at 170 °C and 225 °C (Fig. 1b and c) making the grains well connected as compared to that of as deposited film shown in Fig. 1a. About 15–20 nm peak to peak height in roughness profile is observed for film annealed at 225 °C, while it is only about 4–5 nm for as deposited film, indicating presence of voids. This could be due to desorption of some CuPc molecules since organic materials are known to re-evaporate under annealing [2,13,14].

XRD pattern of CuPc films annealed at different temperatures are shown in Fig. 2. Peak corresponding to (200) plane of metastable α phase CuPc is observed for the as deposited films and after annealing at 170 °C (devices 1 and 2). Peaks corresponding to (100) planes of β phase is observed for the film annealed at 225 °C (device 3) [7]. After annealing at 225 °C, conversion from α to β phase might partly be occurring as seen by a small peak at 6.9° which could be due to the peak corresponding to (200) plane of α phase CuPc. Presence of (200) and (100) peaks indicate edge on configuration arrangement of CuPc molecules with their stacking axes parallel to the substrate surface. This arrangement leads to π–π stacking in the direction of current which helps in efficient transport of charge carriers along the channel. It is well known that

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