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Transistor level fault diagnosis in digital circuits using artificial neural network



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ABSTRACT

In the design of digital circuits, transistor level faults occur due to open or shorted connection in the transistor terminals and with the variations in the transistor parameters. In this study fault diagnosis for hard faults in the digital circuits using artificial neural network and virtual instrument is presented. During the diagnosis process the parametric variations in transistors are also taken into account by varying the threshold voltages of the transistors. The output responses of the circuit under test under faulty and fault free conditions are plotted for all the input combinations. The resulting responses are curve fitted using polynomial curve fitting. The polynomial coefficients are used as signatures values to train the back propagation artificial neural network, which in turn is used for fault classification. The virtual instrument is designed to implement the fault diagnosis system. The system is validated with experiments on universal gates and all the proposed faults are correctly diagnosed.

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1. Introduction

The CMOS design of the digital circuits is affected by different types of permanent faults; these include hard faults and the parametric faults. Hard faults are categorized as stuck-at faults (stuck-0, stuck-1), transistor level faults (transistor open, transistor short), delay faults (gate delay, path delay), leakage faults (IDDQ), interconnection faults (bridging, open, coupling). The transistor parametric faults occur due to the change in the threshold voltage of the transistor and due to change in the *W/L* ratio of the transistor. Many studies have been presented for the fault diagnosis in digital circuits with different fault models. The delay path faults are considered in [1]. The test calculation algorithm is proposed for fault diagnosis using multiple paths. The stuck at faults diagnosis reported in [2] uses

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http://dx.doi.org/10.1016/j.measurement.2015.12.045 0263-2241/© 2015 Elsevier Ltd. All rights reserved. the algorithm implemented FPGA. The stuck at faults occurring due to coupling along with the short faults are discussed [3]. A simulation study based on the path delay for fault detection in the digital circuits is presented in [4]. In this increase in simulation efficiency is also reported. Threshold model of the circuit is used to distinguish between the acceptable and non acceptable faults in the circuit. This model is used to diagnose the stuck at faults [5]. The method [6] proposed the built in sensor for the detection of open and short circuit faults. A sensing element is connected in parallel with the circuit nodes for fault detection. In [7] a fault diagnosis method based on artificial neural networks for multiple stuck at 0 and stuck at 1 fault is given. This method converts the multiple faults into single fault by adding additional gates. Simulation technique [8] also describes the stuck at faults. Hard fault diagnosis for the PLL loop using back propagation neural network are reported in [9]. A two level approach [10] for the fault diagnosis in digital circuit reduces the complexities due to the large fault dictionaries. The parametric



variations in the CMOS circuits generally cause the delay faults; a DFT technique [11] presents fault diagnosis in high performance digital circuit. A gate level stuck at faults using modeling [12] with a buffer attached to the gate, also increase the performance of the diagnosis process. A hierarchal approach from macro level to gate level [13] for the stuck at fault is given. It has been observed that every method describes their best diagnosis efficiency. The hard fault diagnosis in digital circuits with the parametric variations in the transistor design needs to be addressed.

In this study we present the transistor level hard faults in digital circuits with the parametric variation in transistor threshold voltage. Various open and short circuit faults of the transistors are modeled. The circuit under test is simulated for each fault model and the fault free state of the circuit for all the possible combinations of the digital input. The simulation results are obtained for every fault model with the variation in the threshold voltages of the transistors. The responses of the circuit recorded are curve fitted with polynomial curve fitting. The uniqueness in the polynomial coefficients for each fault model provides the basis of the fault diagnosis. A back propagation artificial neural network is trained with the polynomial coefficients does the fault classification. The virtual instrument of the fault diagnosis system is designed using graphical programming in LabVIEW [14]. Two benchmark digital circuits namely two input NAND and NOR gates are used in the study for fault diagnosis to validate our method. The experimental results are presented for the single hard fault diagnosis and it has been observed that faults are diagnosed correctly with good accuracy.

2. Proposed method

The fault diagnosis is categorized into four steps: circuit response measurement, preprocessing, fault classification and design of virtual instrument. The variation caused in the circuit responses under fault and fault free conditions leads to the fault classification. The single open and short circuit faults are considered in this study under the varying threshold voltage parameter of the transistors.

2.1. Circuit response measurements

The response of the digital circuit is obtained by applying two different pulse trains at their inputs such that all the possible input combinations are met. The circuit is simulated for all the open and short circuit fault models with variation in the threshold voltage. The effect of the threshold voltage on the response of the circuit is obtained by the Monte-Carlo analysis. Each run of the Monte-Carlo analysis gives change in the output response of the circuit for each fault model. This variation in the response leads to the fault diagnosis process.

2.2. Preprocessing

The response data is collected after the Monte-Carlo simulations for each of the defined fault model. We have different circuit response waveforms indicating the responses for each Monte-Carlo run. The data collected from these different responses is preprocessed using polynomial curve fitting. The proper and distinguishable features in the form of polynomial coefficients are obtained using curve fitting.

The estimated values of the polynomial coefficients are obtained by the least squares method which in turn minimizes the summed square of residuals. The response data $(x_1,y_1), (x_2,y_2), \ldots, (x_k,y_k)$ is approximated using least squares *j*th polynomials method. The least-squares *j*th degree Polynomials method uses *j*th degree polynomial $y = a_0 + a_1x + a_2x^2 + \ldots + a_jx^j$ where $k \ge j + 1$. According to the Legendre's principle of least square errors, the minimum value of sum of squares of error, represents the best curve fit. The sum of square of errors *E* will be minimum for the best fitting curve f(x).

$$E = \sum_{i=1}^{k} [y_i - f(x_i)]^2$$

= $\sum_{i=1}^{k} [y_i - (a_0 + a_1 x_i + a_2 x_i^2 + \dots a_j x_i^j)]^2 = \min$ (1)

where in (1) x_i and y_i are known values. $a_0, a_1, a_2, \ldots, a_m$ are unknown coefficients. These unknown coefficients will yield their first derivative zero for least square error.

$$\begin{cases} \frac{\partial E}{\partial a_0} = 2\sum_{i=1}^{k} \left[y_i - \left(a_0 + a_1 x_i + a_2 x_i^2 + \dots a_j x_i^j \right) \right] = 0 \\\\ \frac{\partial E}{\partial a_1} = 2\sum_{i=1}^{k} x_i \left[y_i - \left(a_0 + a_1 x_i + a_2 x_i^2 + \dots a_j x_i^j \right) \right] = 0 \\\\ \vdots \\\\ \frac{\partial E}{\partial a_j} = 2\sum_{i=1}^{k} x_i^j \left[y_i - \left(a_0 + a_1 x_i + a_2 x_i^2 + \dots a_j x_i^j \right) \right] = 0 \end{cases}$$
(2)

After the expansion of the above equations, in (2) we have

$$\begin{cases} \sum_{i=1}^{k} y_i = a_0 \sum_{i=1}^{k} 1 + a_1 \sum_{i=1}^{k} x_i + \dots + a_j \sum_{i=1}^{k} x_i^j \\ \sum_{i=1}^{k} x_i y_i = a_0 \sum_{i=1}^{k} x_i + a_1 \sum_{i=1}^{k} x_i^2 + \dots + a_j \sum_{i=1}^{k} x_i^{j+1} \\ \vdots \\ \sum_{i=1}^{k} x_i^j y_i = a_0 \sum_{i=1}^{k} x_i^j + a_1 \sum_{i=1}^{k} x_i^{j+1} + \dots + a_j \sum_{i=1}^{k} x_i^{2j} \end{cases}$$
(3)

The polynomial coefficients a_0, a_1, \ldots, a_j can be obtained by solving these above given (3), linear equations. Polynomial curve fitting is done using the curve fitting tool of LabVIEW software. Which is also based on the theory of least square methods. Since the frequency response graphs are different for different fault models, polynomial coefficients are also different and unique for different faults. The fault dictionary is prepared using these polynomial coefficients for fault classification.

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