Sensors and Actuators A 216 (2014) 158–166

Contents lists available at ScienceDirect

Sensors and Actuators A: Physical

journal homepage: www.elsevier.com/locate/sna

Development of highly-sensitive and ultra-thin silicon stress sensor chips for wearable biomedical applications

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ARTICLE INFO

Article history:
Received 27 April 2014
Received in revised form 17 May 2014
Accepted 17 May 2014
Available online 27 May 2014

Keywords:
Ultra-thin stress sensor chip
Wearable sensor
Thinning
Pulse measurement
Othodontic force

ABSTRACT

This paper reports the development of a highly-sensitive and ultra-thin silicon stress sensor chip (UTSC) and its applications for wearable sensors. Stress sensor chips are fabricated using CMOS technology, and after dicing the individual chips are reconfigured into a virtual wafer on a carrier wafer using temporary adhesive bonding. The reconfigured wafer is then thinned using mechanical grinding, polishing, and wet etching. After thinning, the sensor chips with thickness of 35 μm are laminated to a thin Kapton PI film, followed by de-bonding to separate the carrier wafer. Measurement results show that the UTSC is able to comply with curved surfaces, and the sensitivity is around 70 times that of metal strain gauge. The specifications of the UTSC are characterized in terms of linearity, repeatability, hysteresis, and zero drift. The UTSCs are demonstrated to measure human pulses on wrist and orthodontic forces of invisible aligners for dental treatment. The preliminary results show that the reconfigured method is applicable to thinning individual chips, and the UTSCs are flexible and sensitive enough for measurement of stress and strain on curved surfaces on human bodies.

1. Introduction

In the last decade tremendous progress has been made on development of wearable and implantable sensors for health monitoring, disease treatment, environment monitoring, as well as consumer electronics and industrial measurement [1–5]. Most wearable sensors employ organic polymer materials as the substrate to provide flexibility, whereas the sensing elements are either deposited/grown directly on the polymer substrate or transferred from other (most silicon) substrates.

For direct deposition, different deposition methods, including chemical vapour deposition (CVD) [6], physical vapour deposition (PVD) [7,8], screen- and ink-printing [6,9], have been used to fabricate a large variety of sensing materials and structures, such as metals [8,10], nanorods and nanoparticles [6,11,12], polysilicon thin film transistors [13–15], carbon nanotubes [16], on various polymer substrates such as poly(vinilidene fluoride) (PVDF) [7], polyethylene terephthalate (PET) [6,11], polyimide [12,17], parylene [10], etc. Direct deposition has the advantages of ease of fabrication and low cost. However, organic materials typically result in devices with poor life-time and low charge carrier mobility [18]. Therefore, direct deposition is suitable for the sensors of which the performance does not depend on charge carrier mobility.

For the sensors relying on fast carrier mobility, wafer transfer is preferred, in which silicon sensor wafers are diced, thinned, and laminated to a polymer substrate after they are fabricated using complementary-metal-oxide-semiconductor (CMOS) or microelectromechanical system (MEMS) technologies [19–21]. So far, various fabrication methods have been developed [22–27] to achieve wafer transfer, which can be classified into dicing-before-thinning, dicing-after-thinning, and dicing-by-thinning according to the sequence of thinning relative to dicing. For dicing-before-thinning [22–24], the silicon wafers with sensing elements are diced into single chips, and then the individual chips are thinned and laminated with a flexible substrate. For dicing-after-thinning [24,25], the whole wafer is firstly thinned from the backside and then is diced into chips before or after laminated with a polymer substrate. For dicing-by-thinning [28,29], mechanical grinding is used to thin a wafer from the backside and automatically singulate the wafer into chips with the assist of the grooves etched or sawed on the front side prior to thinning. Despite of the high mobility of

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http://dx.doi.org/10.1016/j.sna.2014.05.018
0924-4247/

silicon, the ultra-thin sensor chips are fragile and impose a great technical challenge to processing.

Although direct deposition on polymer substrates is popular, it is not a universal technology and some physical sensors, such as flow sensors [19], shear stress sensors [21], CMOS image sensors [30], and stress/strain sensors [31], prefer to wafer transfer to exploit the high mobility for high performance. Stress sensors are a critical wearable sensor for measurement of heart beat, blood pressure, pulse, and force of bones and soft tissues [32,33]. Different flexible stress sensors have been developed using poly- and nano-crystalline silicon piezoresistors [34,35], single crystalline silicon piezoresistors [31,36], or carbon nanotube composites [37]. Single crystalline stress sensors are highly sensitive [35] and allow many measurements that are impossible with thick stress sensors to be reality. For example, measurement of tooth orthodontic force requires a flexible, ultra-thin, and highly-sensitive stress sensor because of the small orthodontic force (around 1 N) and the limited space between the brackets and the curved tooth surface [38,39].

This paper reports the development of an ultra-thin stress sensor chip (UTSC) using wafer transfer technology and its biomedical applications. UTSCs with thickness less than 50 μm have good flexibility to withstand a high bending level to conform to curved surfaces of human bodies [3]. To fabricate UTSCs, individual chips are reconfigured as a virtual wafer using temporary chip-to-wafer bonding, and the reconfigured wafer is then thinned from the backside, followed by transfer to a flexible substrate. The UTSCs, about 70 times more sensitive than metal strain gauge (MSG), are demonstrated to measure pulse on wrist and orthodontic force.

2. Sensor design and fabrication

A UTSC is a laminated structure consisting of a flexible polymer substrate and an ultra-thin silicon sensor chip fabricated using CMOS technology and reconfigurable backside thinning. The fabrication processes include the following steps. (1) Temporarily bonding normal sensor chips fabricated in a CMOS foundry to a carrier wafer using temporary bonding adhesive to reconfigure a virtual wafer. (2) Thinning the reconfigured wafers from the backside using mechanical grinding, polishing, and wet etching. (3) Adhesive bonding the thinned chips to a flexible substrate and releasing the UTSC from the carrier wafer by removing the temporary bonding adhesive. (4) Wire bonding the interconnects.

2.1. Stress measurement

Stress measurement is implemented using metal-oxide-semiconductor field-effect-transistors (MOSFET) by exploiting the piezoresistive effect [41], as shown in Fig. 1. Stresses applied to the substrate of a MOSFET change the mobility of electrons and holes in the transistor channels. The current outputs of P- and N-MOSFET with different angles with respect to the wafer crystalline coordinate are sensitive to different stress components [42]

$$\frac{\Delta I_{90^\circ}}{I_{90^\circ}} - \frac{\Delta I_{0^\circ}}{I_{0^\circ}} = \pi_{44}^{P}\left(\sigma'_{11} - \sigma'_{22}\right) \quad (1)$$

$$\frac{\Delta I_{45}}{I_{45}} - \frac{\Delta I_{-45}}{I_{-45}} = -2(\pi_{11}^{n} - \pi_{12}^{n})\sigma_{12} \quad (2)$$

where I and ΔI are the current outputs and the corresponding changes, the subscripts of the current represent the angles of the channels with respect to the silicon crystalline coordinate, π_{11}, π_{12}, and π_{44} are the components of the piezoresistive coefficients, the superscripts of the coefficients represent P- and N-type, σ_{11} and σ_{22} are the in-plane normal stress components, and σ_{12} is the shear stress component.

The test UTSC consists of 256 MOSFET stress cells arranged in a 16×16 array configuration. Each cell includes a pair of NMOS cascade current mirrors and PMOS cascade current mirrors. The NMOS current mirrors are aligned to $\pm 45^\circ$ with respect to the silicon crystalline coordinate, and the PMOS current mirrors are $0^\circ/90^\circ$. Therefore, each cell can measure the difference in the two normal stresses and the shear stress using the P- and N-MOSFET, respectively. Each cell is addressed using row- and column-selection circuits, and the output is amplified with an off-chip circuit. The stress chips were fabricated using UMC 0.18 μm CMOS technology, and the size of each cell is 55 μm × 55 μm.

When subject to external bending, in-plane stresses are induced in the sensor chip. The normal in-plane stress caused by bending can be roughly expressed as

$$\sigma_{11} = \frac{z \cdot M}{I_z} = \frac{6M}{bh^2} \quad (3)$$

where z is the interval between the device surface and the neutral plane, M is the external bending moment, I_z is the moment of inertia, b and h are the chip width and thickness, respectively.

It is clear that the normal stress is inversely proportional to the square of the chip thickness. As the output of P-MOSFET is linear with the normal stress, the sensitivity for stress measurement is highly dependent on the thickness of the sensor chip. Thus thinning the sensor chips can significantly increase the normal stress and thus the sensitivity.

2.2. Reconfiguration of individual chips

The major drawback of thinning a single chip from the backside using mechanical grinding is the low efficiency and the low yield. In addition, mechanical grinding may induce micro cracks around the chip edges. Such defects are insignificant for chips with normal thickness, but become severe for ultra-thin chips because they tend to extend to the whole thickness and cause chip crack. The proposed reconfiguration method is able to improve the thinning efficiency and avoid micro cracks.

The individual stress senor chips from foundry have a dimension of 2 mm × 2 mm and a thickness of 300 μm. Before thinning, the chips are temporarily bonded to a carrier wafer in a manner of tightly packed array, as shown in Fig. 2(a). First, a temporary bonding adhesive, Wafer Bonder HT10.10 (Brewer Sciences Inc.), is spin-coated on the carrier wafer with a thickness of 7 μm. Second, the individual chips are placed onto the bonding adhesive side by side, and 4 protection silicon chips with similar thickness to the sensor chips are placed surrounding the chip array. Then, the sensor chip array together with the protection chips is bonded at 180 °C.

The temporary adhesive bonding, which reconfigures individual chips into a virtual wafer on the carrier wafer, achieves high bonding strength for thinning and is easy to de-bond [40], enabling high processing efficiency by thinning multiple chips simultaneously instead of one by one. The protection chips prevent the surrounded chips from being damaged by extending the chip boundaries and providing identical surfaces. The small gaps between the sensor chips and the protection chips are filled with the temporary bonding adhesive, such that the sharp edges of the sensor chips are further protected to avoid the damage from mechanical grinding. It is important to note that the sensor chips on the carrier wafer should be symmetrical to the wafer center, so that the pressure in mechanical grinding and polishing is uniformly exerted on each sensor chip to obtain uniform thinning rate.

2.3. Thinning reconfigured wafers

After being reconfigured into a virtual wafer, the sensor chips are thinned from the backside using mechanical grinding, polishing,