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The hysteresis-free negative capacitance field effect transistors using non-linear poly capacitance ☆

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ABSTRACT

A gate structure design for negative capacitance field effect transistors (NCFETs) is proposed. The hysteresis loop in current–voltage performances is eliminated by the nonlinear C–V dependence of polysilicon in the gate dielectrics. Design considerations and optimizations to achieve the low SS and hysteresis-free transfer were elaborated. The effects of gate-to-source/drain overlap, channel length scaling, interface trap states and temperature impact on SS are also investigated.

1. Introduction

Steep-slope transistors with subthreshold slope (SS) < 60 mV/dec can reduce the power consumption [1–3]. Ferroelectric (FE) negative capacitance has been demonstrated to step up voltage and thus to reduce SS lower than 60 mV/dec [4].

According to the Landau theory [5], ferroelectric material has a S-shape polarization–electric field characteristics in which the negative $\frac{dP}{dE}$ represents the negative capacitance. However, the negative slope segment is energetically unstable in a single ferroelectric capacitor. It also leads to a hysteresis jump in the polarization [6]. In order to effectively utilize the ferroelectric negative capacitance, an ordinary dielectric have to be in series with ferroelectric such that the overall capacitance is still positive [7,8]. Therefore, the ferroelectric negative capacitance region is stabilized and the hysteresis loop vanishes. To have significant reduction of SS, the magnitude of FE capacitance should be as close as the MOS capacitance theoretically [9].

Some NCFETs, although achieving sub-60 mV/dec SS, cause hysteresis in the current–voltage performance. Works have been done to control the trade-off between SS reduction and hysteresis-free [10,11]. Also, theoretical analyses [12–14] of a metal-ferroelectric-semiconductor FET without oxide were previously reported to optimize SS. The addition of oxide (Fig. 1(a)) to prevent the PZT diffusion into channels were demonstrated to have steep slope. Very recently, hysteresis-free NCFETs has been reported [15] experimentally.

In this work, a polysilicon-FE gate capacitance is proposed to add on the original MOS capacitance, to achieve the positive total capacitance, but itself remains negative. A hysteresis-free and sub-60 mV/dec SS transfer curve is achieved.

2. Device structure concept

The proposed gate stack consists of n-type polysilicon, FE, and ordinary oxide (Fig. 1(a)). The interface trap density (D_{it}) at the oxide/semiconductor interface is considered. Charge configurations of each layer under external positive bias are also shown. Q is the charge density, and Q_p is the induced polarization charge density in the ferroelectric layer, where the electric dipole moment P directs downward. The Ge channel is expected to be adopted in

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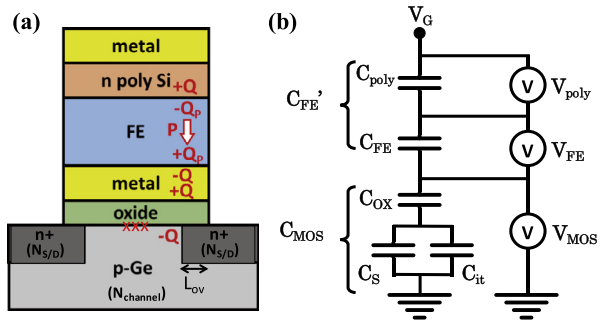

Fig. 1. (a) Schematic cross-sectional view of a NCFET using polysilicon-FE gate stack. L_{ov} is the overlapping length between source/drain and the gate. $N_{S/D}$ and $N_{channel}$ are the $n+$ source/drain doping concentration and p-substrate doping concentration, respectively. (b) An equivalent capacitance model of a NCFET using polysilicon-FE gate stack.

industry [16,17] before NC gate structures. Similar results are also obtained for Si channels.

Fig. 1(b) shows the equivalent capacitance model. The MOS capacitance (C_{MOS}) is the series combination of the oxide capacitance (C_{ox}) and the sum of semiconductor capacitance (C_s) and interface traps capacitance (C_{it}). The polysilicon (C_{poly}) in series with FE (C_{FE}) provides a negative equivalent ferroelectric capacitance ($C'_{FE} = (1/C_{FE} + 1/C_{poly})^{-1}$), which is nonlinear as a function of gate voltage and its magnitude approaches to MOS capacitance closely at the subthreshold region.

A floating metal layer [18–20] is placed between gate oxide and FE to unify the potential profile along channel [21,10]. The equipotential metal surface keeps the ferroelectric behavior to be controlled only by gate voltage, rather than forming multi polarization domain under 2-dimensional electric field. Therefore, Landau theory in 1-dimensional single polarization domain could be valid to describe the FE polarization. Also, works have been done to prove that metal/ferroelectric/polysilicon/insulator/Si (MFPIS) [22–24], metal/ferroelectric/metal/insulator/Si (MFMIS) [25,26], and metal/ferroelectric/metal/polysilicon/insulator/Si (MFMPIS) [27,28] can efficiently suppress the depolarization field in the ferroelectric layer.

3. Simulation methodology

After simulating the original $I_D - V_{MOS}$ curve of the MOSFET part using *TCAD tools* [29], the oxide electric field (E_{OX}) at given MOSFET voltage (V_{MOS}) can be extracted. $PbZr_{0.5}Ti_{0.5}O_3$ as the ferroelectric material is used in our study. The displacement continuity at the boundary between gate oxide and ferroelectric [30] leads to Eq. (1):

$$\varepsilon_{ox} \cdot E_{ox} = \varepsilon_0 \cdot E_{FE} + P, \tag{1}$$

where P denotes the polarization charge per unit area in FE and E_{FE} is the electric filed in FE.

The Landau theory between E_{FE} and P is [31–33]:

$$E_{FE}(P) = 2\alpha P + 4\beta P^3 + 6\gamma P^5, \tag{2}$$

where Landau parameters ($\alpha = -4.887 \times 10^9$ cm/F, $\beta = 4.764 \times 10^{17}$ cm^5/C^{2}F, $\gamma = 1.336 \times 10^{26}$ cm^9/C^{4}F) of $PbZr_{0.5}Ti_{0.5}O_3$ are adopted from [31–33]. Then, P can be solved from Eqs. (1) and (2).

Moreover, for a given ferroelectric thickness (t_{FE}), the voltage across the ferroelectric (V_{FE}) is derived from

$$V_{FE}(P) = t_{FE} \cdot \left(2\alpha P + 4\beta P^3 + 6\gamma P^5\right). \tag{3}$$

On the top of the ferroelectric layer, the voltage drop on polysilicon (V_{poly}) is equal to polysilicon surface potential (φ_s). Therefore, for a given inversion charge density (Q_{inv}), we can derive V_{poly} from [34]:

$$Q_{inv} \approx \sqrt{2\varepsilon_{si} kTN_{poly}} \left[\left(\frac{-qV_{poly}}{kT} - 1 \right) + \frac{n_i^2}{N_{poly}^2} \left(e^{-\frac{qV_{poly}}{kT}} - 1 \right) \right]^{\frac{1}{2}}. \tag{4}$$

By summing up each voltage obtained [35], the corresponding gate voltage is:

$$V_G = V_{MOS} + V_{FE} + V_{poly}. \tag{5}$$

Therefore, the relationship between charge density and voltage across each layer could be obtained (Fig. 2(a)). The hysteresis loop of the NCFET mentioned in Section 1 was observed (Fig. 2(b)). The hysteresis jump occurs from A to B while the voltage sweeps in positive direction. Likewise, when voltage sweeps backward, the charge jumps from C to D. However, after applying the polysilicon layer on top of FE, the negative capacitance region does not exist anymore (the green Q *v.s.* V_G curve in Fig. 2(a)).

A further improved model with the interface states at oxide/semiconductor is investigated [36]. The oxide/semiconductor interface charge density can be expressed as:

$$Q_{it} = -q \int_{E_0}^{+\infty} F(E)dE + q \int_{-\infty}^{E_0} [1 - F(E)] D_{it}(E)dE, \tag{6}$$

where $F(E)$ is Fermi–Dirac distribution, and E_0 is the charge neutrality level. As a result, Eq. (1) can be rewritten as

$$Q_s + Q_{it} = \varepsilon_{ox} \cdot E_{ox} = \varepsilon_0 \cdot E_{FE} + P. \tag{7}$$

In order to find the parameters achieving optimized SS [12] with non-hysteresis operation, an equivalent capacitance model (Fig. 1(b)) is used to illustrate the design concepts. The capacitances of each layer are shown in Fig. 3.

For an NCFET, SS can be formulated as

$$SS = 60 \times \left(1 + \frac{C_s + C_{it}}{C_{ins}}\right) = 60 \times \left(1 + \frac{C_s + C_{it}}{C_{ox}} - \frac{C_s + C_{it}}{|C_{FE}|}\right). \tag{8}$$

$|C_{FE}|$ must be smaller than C_{ox} to ensure SS < 60 mV/dec.

Now, the impact of ferroelectric gate stack is considered as a voltage amplification. The voltage gain (A_V) is defined by the original MOSFET voltage (V_{MOS}) with respect to the gate voltage (V_G) of NCFET. As elaborated in [21], SS can be formulated as below:

$$SS = \frac{\partial V_G}{\partial (\log I_d)} = \frac{\partial V_{MOS}}{\partial (\log I_d)} \frac{\partial V_G}{\partial V_{MOS}} = 60\left(1 + \frac{C_s + C_{it}}{C_{ox}}\right)\frac{1}{A_V}, \tag{9}$$

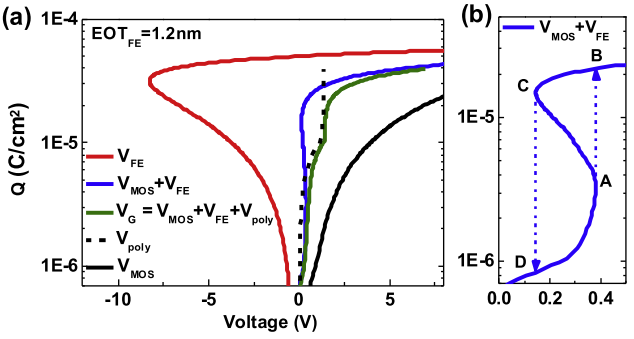

Fig. 2. (a) The relationship between the charge density and the voltage drop on the different combination of layers in a NCFET with polysilicon-FE gate stack. ($EOT_{FE} = 1.2$ nm, $N_{poly} = 2 \times 10^{20}$ cm^{-3}). (b) The close-up of the blue curve in (a), which is the Q-V curve of a hysteretic NCFET. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)