Solid-State Electronics 113 (2015) 151–156

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Reliability study of organic complementary logic inverters using constant voltage stress

N. Wrachien [a,*], A. Cester [a,1], N. Lago [a,1], A. Rizzo [a,1], R. D'Alpaos [b,2], A. Stefani [b,2], G. Turatti [b,2], M. Muccini [b,c,2], G. Meneghesso [a,1]

[a] Department of Information Engineering, University of Padova, via Gradenigo 6/B, 35131 Padova, Italy
[b] E.T.C. S.r.l., via Piero Gobetti, 101, 40129 Bologna, Italy
[c] CNR-ISMN Bologna, via Piero Gobetti, 101, 40129 Bologna, Italy

ARTICLE INFO

Article history:
Available online 6 June 2015

Keywords:
Organic Thin-Film Transistors
Reliability
Bias stress
Logic inverter

ABSTRACT

We performed constant voltage stresses with different bias conditions on all-organic complementary inverters. We found a 20% maximum variation of DC inverter parameters after a 10^4-s stress. However, the largest stress-induced degradation was found in the delay times, which increased by a factor as high as 7. This is mainly due to the threshold voltage variation of the p-type thin-film-transistor and the mobility reduction of the n-type thin-film transistors, which both decrease the saturation drain current.

1. Introduction

Progresses on Organic-Thin-Film-Transistors (OTFTs) made them a promising low-cost alternative to a-Si TFTs [1,2]. Organic devices have many advantages with respect to their silicon counterparts. In fact, organic materials can be inexpensively deposited using many techniques, such as spin-coating or ink-jet printing [3,4]. Those processes require much lower temperatures than those required for silicon deposition, allowing the growth of organic semiconductors over plastic substrates. Plastic substrates, in turn, are flexible, much lighter, more robust to mechanical deformation and cheaper than glass, allowing the integration of organic electronics in many fields. For instance, OTFTs could be employed in RF-IDs, flexible displays, smart textiles, sensors, etc. In many of these applications, a relatively low operating frequency is required, and they are mainly battery or near-field powered. The limited energy/power budget makes complementary logic a desirable choice to cut down power requirements, because static power dissipation is minimized, while dynamic power is relatively small, due to the low operating frequency. Complementary logic also features better noise margins, with respect to nMOS- or pMOS-only logic.

Unfortunately, OTFTs still have some drawbacks especially in terms of stability and reliability. In fact, OTFTs are very sensitive to air and humidity exposure [5,6], and their characteristics change under illumination, with bias and with temperature [7]. Many works in the literature have addressed the OTFT stability and reliability under electrical stress [7–12], light [7,11–13] and ultraviolet exposure [14–18].

Some works also already addressed the characterization of inverters with complementary OTFTs [19–21], or analyzed the bias effects on the DC inverter characteristics with only p-type or n-type OTFTs [22,23]. Very few works [24,25] also provided some results on bias effects on the DC characteristics of complementary inverters. However, our work represents the first systematic investigation of the reliability of inverters with all-organic complementary thin-film-transistors, using accelerated electrical stress. Our analysis not only includes the most important static OTFTs and inverter parameters, but also includes for the first time the propagation delay variation, never considered before in the reliability study of OTFT-based inverters.

2. Experimental and devices

Throughout this work, we analyzed complementary inverters with p-type and n-type OTFTs, whose cross section is shown in Fig. 1a. Devices were fabricated in Bottom Gate – Top Contact configuration, on glass substrates with gate contact consisting of a 150 nm thick ITO layer. A 450-nm Poly(methyl methacrylate) (PMMA) layer was spin-coated on top of ITO as dielectric layer. A 20-nm thick semiconductor layer was deposited by physical vapor deposition at 0.015 nm/s. The n-type and p-type layers were Diperfluorohexyl-Quaterthiophene (DFH-4T) and Dihexyl-Quaterthiophene (DH-4T), respectively [26]. Finally, 70-nm thick gold drain and source electrodes were deposited on top of the stack

* Corresponding author. Tel.: +39 049 827 7600; fax: +39 049 827 7699.
[1] Tel.: +39 049 827 7600; fax: +39 049 827 7699.
[2] Tel.: +39 051 6398521; fax: +39 051 6398540.

http://dx.doi.org/10.1016/j.sse.2015.05.028
0038-1101/

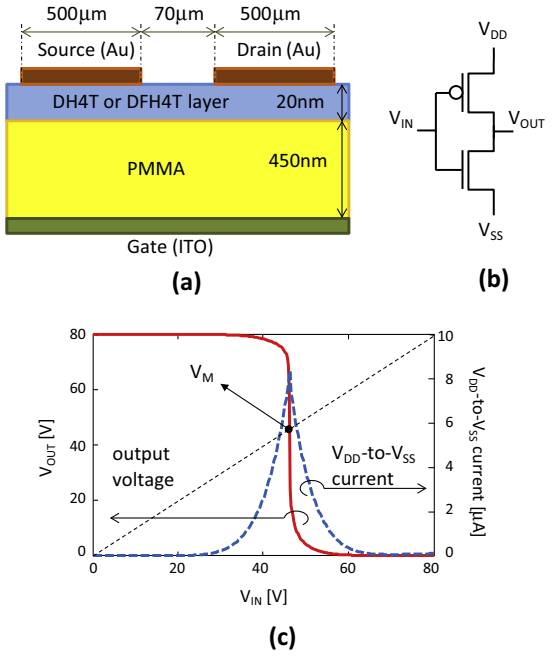

Fig. 1. (a) Cross section of n-channel (DFH4T) and p-channel (DH4T) organic TFT used in this work. (b) Inverter schematics with signal names, which will be used throughout this work. (c) Typical transfer characteristics (left scale) and direct path current (right scale) of the inverters used in this work.

at 0.1 nm/s. OTFTs' channel width was 12 mm, while channel length was 70 µm. The devices are encapsulated with glass covers, to avoid degradation due to air exposure. Electron mobility of the n-type OTFTs (nTFTs) is 0.28 $cm^2 V^{-1} s^{-1}$ and hole mobility of the p-type OTFTs (pTFTs) is 0.09 $cm^2 V^{-1} s^{-1}$, before stress.

The stress procedure consists of a Constant Voltage Stress (CVS), which is periodically interrupted to perform characterizations. The CVS is performed with different biases and connection, which are summarized in Table 1. Fig. 1b shows the inverter schematics with the signal naming conventions, which will be used in this work. The connections, named SH, SL, and SAT, emulate some of the different inverter operating conditions. In SH the inverter is stressed with the input held at the logic level high (nTFT is in the ON state, the pTFT is in the OFF state). In the SL configuration, the input is held at the logic level low (nTFT is in the OFF state, the pTFT is in the ON state). In SAT connection, the bias configuration is chosen so that both transistors are conducting the saturation current and each OTFT is stressed with $|V_{DS}| = |V_{GS}| = 100$ V. This particular configuration has been chosen to emulate the degradation, which occurs just after the rising and the falling edges of the input voltage, when the inverter is loaded with a large capacitance. In fact, when the input goes from "1" to "0", the nTFT will turn-off in a relatively short time. The pTFT also turns on, but, because of the large capacitive load, its V_{DS} will remain close to $-V_{DD}$, for a relatively long time, depending on the capacitive load. Consequently, the pTFT will be subjected for a relatively long time to a large $|V_{DS}|$ with $V_{GS} = -100$ V. A similar condition occurs on the nTFT during the "0" to "1" transition (of course, with opposite V_{GS} and V_{DS} polarities).

In SH and SL the power supply voltage is 100 V to accelerate the degradation. In SAT, the $|V_{DD} - V_{SS}|$ voltage is 200 V, but each transistor is stressed with $|V_{DS}| = |V_{GS}| = 100$ V.

Characterizations considered in this work include:

(1) The double-sweep saturation current–gate voltage curve (i.e. the I_D–V_{GS} taken with $V_{GS} = V_{DS}$, I_{SAT}–V_{GS} hereafter) of pTFTs and nTFTs.

Table 1
Stress conditions.

Signal	Stress configuration		
	SH	SL	SAT
V_{DD}	100 V	100 V	100 V
V_{SS}	0 V	100 V	−100 V
V_{in}	100 V	0 V	0 V
V_{OUT}	Open	Open	0 V

(2) The transfer characteristics (I_D–V_{GS}, with $|V_{DS}| = 1$ V).
(3) The double-sweep inverter transfer curve.
(4) The inverter transient step response (taken with a custom compensated 1 GΩ probe to minimize output loading).

A custom low-leakage switch matrix was also developed to allow for the single pTFT or nTFT characterization. Fig. 1c shows the static characteristics and the V_{DD}-to-V_{SS} current of one of the analyzed inverters.

The stress voltage was set to 100 V, in absolute value. Measurement voltage was limited to 80 V. It is worth to note that the voltages are remarkably high, because we are evaluating samples with high-thickness and low-k dielectrics. However, lower operating voltages are easily achievable employing thinner or high-k dielectrics. In a previous work on OTFTs subjected to CVS (see Ref. [27]), we found that, breakdowns apart, the PMMA layer degradation had a smaller impact on the characteristics compared to the degradation of the semiconductor layer. For this reason, in the present work we are focusing only on the effects of the organic semiconductor degradation on the inverter characteristics.

3. Results and discussions

This section is organized as follows: we first show and discuss the effects of electrical stresses at the transistor-level (Section 3.1), then we analyze the effects of OTFT degradation on the inverter characteristics (Section 3.2).

3.1. TFTs

In Fig. 2a–c, we show some selected I_{SAT}–V_{GS} curves measured during the CVS. Insets show a zoom of the curves, to appreciate the small hysteresis in the linear scale, which will be discussed later. In SH, there are very small variations in the pTFT and large degradation in the nTFT. For instance, the saturation drain current exhibit a 70% decrease in the nTFT and less than 10% decrease in the pTFT. The opposite occurs in SL: the pTFT degradation is larger than in nTFT (the saturation drain currents of the nTFT and pTFT decrease of 20% and 50%, respectively). In SAT, i.e. when both TFTs are driving current during stress, both TFTs feature the largest variations (the saturation drain currents decrease of 80% and 45% in nTFT and pTFT, respectively).

Using the trapped-charge-limited current model [28], from the I_{SAT}–V_{GS} and the I_D–V_{GS}, we calculated, the threshold voltage (V_{TH}), and the high electric field mobility (μ). From the subthreshold swing of the I_D–V_{GS} we evaluated the interface trap density variation (ΔN_{IT}).

Fig. 3a–c shows V_{TH}, μ (normalized to the initial value), and ΔN_{IT} evolutions during CVS, plotted as average between the values calculated from the forward and backward sweeps. The evolutions of these parameters suggest different degradation mechanisms in pTFTs and nTFTs, depending on the CVS connections. For instance, the nTFTs mostly exhibit a large μ reduction, especially in SH and SAT (up to 60%), accompanied by large ΔN_{IT} increase. In pTFTs, the parameters are almost unchanged in SH, and μ shows at most a