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Flat single crystal Ge membranes for sensors and opto-electronic integrated circuitry

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ABSTRACT

A thin, flat and single crystal membrane on which to mount sensors is generally required for integration with electronics through standard silicon processing technology. We present an approach to producing single crystal membranes of germanium with in-built tensile strain, which serves to keep the membrane flat and ripple free, and demonstrate a 600 nm thick, free-standing 1 mm^2 Ge membrane. We convert the fabrication technique into an integrated-circuit compatible wafer scale process to produce 60 nm thin membranes with large areas of 3.5 mm^2. The single crystal Ge membrane provides an excellent platform for further epitaxial growth or deposition of materials.

1. Introduction

Integration of all manner of sensors, devices and transducers onto a single chip is coined "system-on-a-chip" [1]. A variety of applications such as accelerometers and gyroscopes, regularly found in today's technology, can be incorporated into these chips but require small scale structures to be fabricated using expensive processing techniques and materials. One of the most common and simple micro-electro-mechanical systems (MEMS) components is the semiconductor membrane, which has been reported with thicknesses down to the order of 10 nm and typical area in the order of 1 mm^2 [2]. Crystalline silicon membranes have also been used for some applications, where membranes are fabricated using multiple expensive steps which may include: ion implantation, bonding, dry etching or electrochemical etching [3,4]. Such membrane fabrication often starts from a silicon-on-insulator substrate which is then subjected to a combination of wet and dry etching [5,6]. However, membranes that survive the process often become warped and are corrugated due to strain within the topmost layers imparted by the buried oxide layer [5]. Other obstacles include membrane layer interdiffusion and the fragile nature of membranes in liquid etchants [2]. Clearly, simplifying the production techniques and making the whole process cheaper would be of great interest.

Silicon membranes are usually fabricated using ion implantation or bonding and dry etching. However, our chosen technique is anisotropic wet etching, since wet etchants are cheaper and simpler than dry etching, a high Si etch rate is possible, and there is the added benefit of the anisotropy which allows crystal planes to be used for etch definition. Si membranes have most commonly been fabricated by etching through a mask layer on the backside of a Si (001) wafer by a wet anisotropic etchant, such as potassium hydroxide (KOH), tetramethylammonium hydroxide (TMAH) or ethylenediamine pyrocatechol (EDP) [7] towards the topside of the wafer where an etch stop layer is defined to protect the membrane layer above. Etch masks or etch-stop layers [8] are frequently made from insulating layers such as SiO_2 or Si_3N_4 and/or highly doped semiconductors where the etch rate significantly drops with increasing dopant concentration [8]. Both the etch stop and masking layers can be the same material, but creating these mask layers requires high temperatures (>600 °C) either to ensure incorporation of a high level of dopant or to grow a good quality dielectric layer that completely resists the etchant. However, if such processes were applied with heterostructures on a membrane, the thermal treatment would result in interdiffusion of the heterostructure, membrane material and substrate, hence ruining the layer definition; consequently, a lower temperature mask is attractive.

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Li et al. [9] used amorphous and polycrystalline Ge layers as mask layers due to the etching selectivity of KOH and TMAH of Si over Ge. They previously reported that polycrystalline Ge has a low etch rate of approximately 0.09 nm min^{-1} within a 42% KOH etchant at 62 °C, whereas it is well known [8] that Si has a relatively high etch rate of approximately 300 nm min^{-1} for similar conditions. Pure Ge can be deposited epitaxially, using either molecular beam epitaxy or chemical vapour deposition (CVD) at temperatures as low as 250 °C where the layer quality is good enough to fully resist alkaline anisotropic etchants, thus solving the problem of low temperature masking. Li et al. also fabricated a Ge membrane, but it was amorphous with corrugations. Consequently, if a low temperature tensile strained crystalline Ge layer could be fabricated (with the tensile strain eliminating the corrugations [10]) it could be the ideal membrane material. In addition, the use of Ge-on-Si would also allow the incorporation of III–V materials [11] on cheap Si substrates that could themselves be turned into membranes. This still leaves the possibility of other applications on membranes such as optoelectronics [12], Ge lasers [13] or even solar cells [14].

Germanium membranes of thickness 1.6 μm have been fabricated by Nam et al. [15] which were then tensile strained to reduce the direct band gap for more efficient light emission, then devices for optoelectronic detection were fabricated on top to demonstrate this effect, later they demonstrated room-temperature electroluminescence with serious implications to Ge lasers [16]. Here, we demonstrate a membrane with the potential for further epitaxial layers to be grown on top so that the advantage of epitaxial heterostructures can be combined with the advantage of fabricating devices on membranes. For example, Fig. 1 shows the theoretically advantageous heterostructure of a compressively strained Ge [17] layer on a reverse graded buffer [18–20], due to the large amount of dislocations in the topmost strained layer dislocation conduction/leakage could still be an issue [21–23]. However, removal of the misfit conduction path could allow the epitaxial layers to artificially become higher in quality so that they could be used for device applications [24], but would need to be kept single crystal and planar for current processing technologies.

Single crystal material has good thermal transport properties compared to poly-crystalline and amorphous materials [25]. This is important for room-temperature MEMS devices, such as accelerometers, gyroscopes and micromirror devices [26]. In the particular case of micromirrors, an essential component in a picoprojector system [27], the surfaces need to be atomically smooth to increase the reflectance of visible light [28]. The need for flat MEMS surfaces is also required for other applications if integration of planar CMOS technology is to be incorporated on membrane-type platforms [4].

The problem of membrane corrugation is thought to be due to strain direction within the layer therefore identical layers of Ge with opposite strain directions could determine the effect on a membrane surface. In a previous study [29], we investigated the thickness dependence of the two temperature Ge growth method for a high quality crystalline layer on Si (001) growth. Ge has a lattice parameter 4.2% larger than Si and in low temperature epitaxial growth the first few monolayers of Ge conform to the Si substrate lattice parameter, which compressively strains the Ge. As the thickness of the layer is increased dislocations form to relieve the strain. A subsequent higher temperature layer enhances this effect until the Ge is 100% relaxed during growth, and is hence strain neutral at this point. However, when cooling from the high growth temperature (>650 °C) the dislocations become immobile, and since Ge has a larger thermal expansion coefficient than Si the Ge lattice parameter will not contract as much as the Si substrate, thereby imparting tensile strain into the Ge layer. From this work, we found conditions to separately create a compressive and tensile strained Ge layer of equal thickness on a Si (001) substrate for membrane fabrication.

2. Experimental procedure and discussion

For this investigation, a double side polished low resistivity (10–25 Ω cm), 4″ silicon (001) wafer of thickness 300 μm Si (001) wafer was used, so that both compressive (c-Ge) and tensile (t-Ge) layers could be grown on either side. Epitaxial growth of the germanium layers was done by reduced pressure chemical vapour deposition (RP-CVD) in an ASM Epsilon 2000E system, using germane as a precursor [19]. Prior to growth, the native oxide of the wafer was desorbed at 1000 °C for 2 min. Initially, the t-Ge layer was grown on the front-side of the wafer, using the two-temperature method, by depositing a 100 nm layer at 400 °C, followed by a 600 nm layer at 670 °C, with a final anneal at 830 °C for 10 min. In order to grow the c-Ge layer on the back-side, the wafer was then cooled to room temperature, unloaded to a nitrogen atmosphere (within a Class 10 clean area), turned over and re-loaded into the growth chamber for a 700 nm deposition at 400 °C. The front-side growth included a higher temperature, so this was performed first to avoid any effect of inter-diffusion on the back-side layer grown at the lower temperature. The wafer turning process was carried

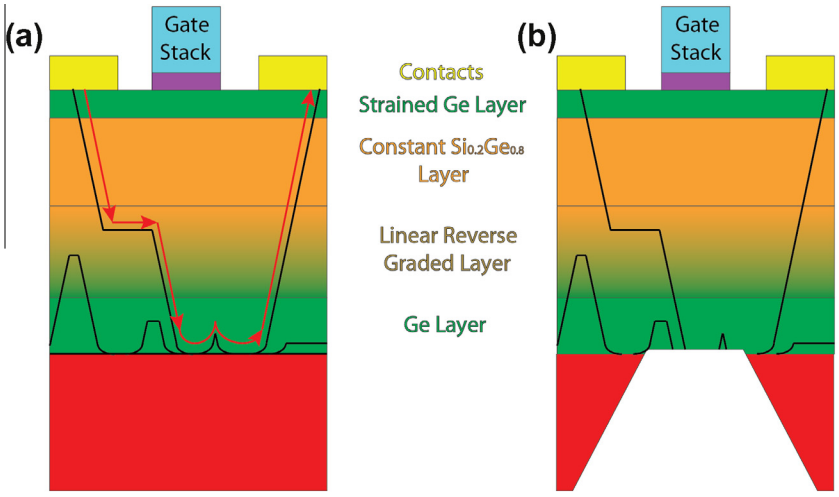

Fig. 1. Shows the possible application of the membranes to incorporate heteroepitaxial layers into their design, this example shows a MOSFET device using a strained Ge layer on a reverse graded buffer. (a) Shows the heterostructure and the possible leakage paths along the dislocations (red), (b) removes these dislocation paths by placing the device onto a membrane. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)