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Research paper

Hopf bifurcation and chaos in a third-order phase-locked loop

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ABSTRACT

Phase-locked loops (PLLs) are devices able to recover time signals in several engineering applications. The literature regarding their dynamical behavior is vast, specifically considering that the process of synchronization between the input signal, coming from a remote source, and the PLL local oscillation is robust. For high-frequency applications it is usual to increase the PLL order by increasing the order of the internal filter, for guarantying good transient responses; however local parameter variations imply structural instability, thus provoking a Hopf bifurcation and a route to chaos for the phase error. Here, one usual architecture for a third-order PLL is studied and a range of permitted parameters is derived, providing a rule of thumb for designers. Out of this range, a Hopf bifurcation appears and, by increasing parameters, the periodic solution originated by the Hopf bifurcation degenerates into a chaotic attractor, therefore, preventing synchronization.

1. Introduction

Since proposed by Bellescize in 1932, the phase-locked loop evolved from being a device mounted with discrete electronic components, to being applied in synchronous frequency demodulation systems [1] in different forms of integrated circuits and software implementations, which are present on computational systems, optics communications devices and even in smart-gride applications [2,3].

Clearly, these different applications correspond to different frequency ranges and synchronism accuracy. However, considering that the PLL architecture is always the same, being described by a closed loop composed of phase-detector (PD), a low-pass filter (F) and a voltage controlled oscillator (VCO), represented in Fig. 1, there are the following possible adjustments to be considered according to the application [4]:

- PD gain and its linearity;
- F frequency response;
- VCO capture range.

The PD is supposed to be nonlinear with the output signal, $v_d(t)$, depending on the sine of the phase difference between the phase of the remote signal, present in the PD input, $v_i(t)$, and the phase of the local oscillation generated by the VCO, $v_o(t)$, since then non small phase errors must be taken into account [5].

The filter that integrates the output of the PD will be considered a second-order low-pass Sallen-Key, with the cut-off frequency normalized to the unity and low-frequency gain given by a variable parameter K that, by construction, is greater

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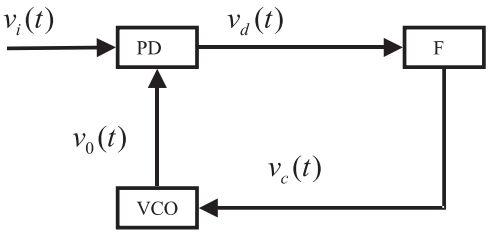

Fig. 1. PLL block diagram.

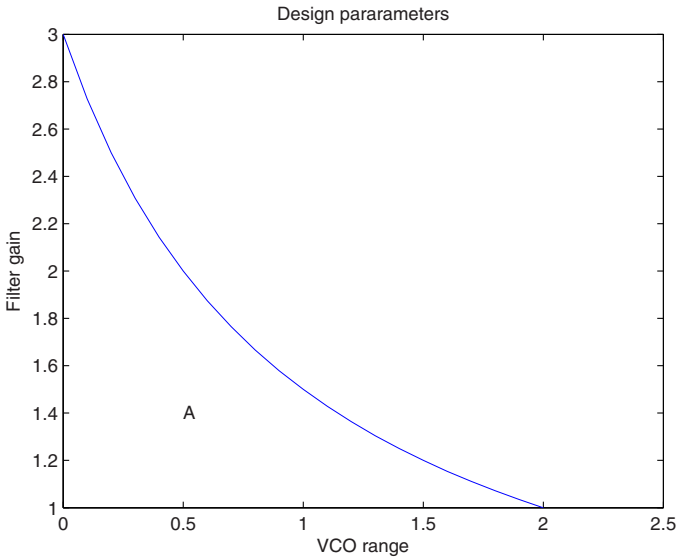

Fig. 2. Parameters design diagram.

or equal to one [6]. The output of the filter, $v_c(t)$, controls the VCO, which its derivative phase is proportional to the filter output [2].

Under these assumptions, the dynamics of the PLL phase-error is described by a third order nonlinear autonomous equation presenting the error-free state as an equilibrium point, which its stability determines how the synchronization system behaves when disturbed.

In spite of having a lot of studies about chaotic behaviors in second-order PLL and for non autonomous input signals [7], the problem concerning third-order autonomous case has been studied only in experimental and numerical ways, considering lag-lead second order filters, showing the onset of chaotic behaviors originated by Hopf bifurcations [8], including a control strategy [9].

Here, the simplest nonlinear PLL architecture, with a multiplier phase detector and an all-pole filter, is studied because it appears in most high frequency applications [10] and the results can be generalized for any filter order [11].

In the next section, the behavior of the third-order PLL will be studied focusing on stable synchronization relating the loop parameters building the hold-in region [12]. This analysis provides a relation between parameters that helps engineers on the design of synchronization systems.

Proceeding it was shown how the limit cycle generated by a Hopf bifurcation appears [14]. Following the reasoning, a new section presents the numerical simulations corresponding to the described situations. As a complement, by using numerical simulation, a route to chaos is presented. The conclusion section finishes the paper.

Other interesting architectures, as Costas loop, are not studied here because they have non continuous models [13], but it could be useful to model the bifurcation cascade related to the constitutive parameters, in order to determine their hold-in range.

2. Hold-in range and design parameters

Considering the described facts and the derivation presented in [6], the PLL dynamical equation to be studied here is:

$$\dddot{\phi} + (3 - K)\ddot{\phi} + \dot{\phi} + KG\sin\phi = 0, \tag{1}$$