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# Fundamental understanding, impact, and removal of boron-rich layer on n-type silicon solar cells

Kyungsun Ryu [a], Chel-Jong Choi [b], Hyomin Park [c], Donghwan Kim [c], Ajeet Rohatgi [a], Young-Woo Ok [a,*]

[a] School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332-0250, USA
[b] School of Semiconductor and Chemical Engineering, Chonbuk National University, Jeonju 561-756, Republic of Korea
[c] Department of Materials Science and Engineering, Korea University, Seoul 136-713, Republic of Korea

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A B S T R A C T

Most boron diffusion technologies result in the formation of an undesirable boron-rich layer (BRL) on the emitter surface. This paper reports on a study of the impact of gradual etching of the BRL on n-type silicon solar cell performance. It is found that gradual removal of the BRL improves surface passivation and bulk lifetime in the finished cell, while over-etching of the BRL results in a sharp decrease in fill factor due to the increased n-factor and series resistance. It is shown that the optimum chemical etching of the BRL formed as a byproduct of the screen-printed boron emitter diffusion used in this study raised the cell efficiency by ~0.5%, resulting in 20.0% efficient large area (239 $cm^2$) n-type solar cells. The change in BRL thickness and morphology as a function of chemical etching time was investigated by TEM and AES measurements to explain the quantitative impact of BRL removal on cell performance.


## 1. Introduction

Current market share of n-type mono-crystalline silicon (Si) for solar cells is only ~5%, however, it has become an active area of investigation in photovoltaics (PV) because of several key advantages over its counterpart p-type Si cells for terrestrial applications. For example, n-type Si has (a) higher tolerance to detrimental metal impurities because of lower capture cross section for holes [1], (b) higher minority carrier lifetime (>1 ms), and (c) absence of light-induced degradation (LID) [2–4] which is known to degrade solar cell efficiency of boron (B) doped p-type Si solar cells by 0.5–1% (absolute) [5]. However, formation of low-cost high performance B emitter has been a barrier for the growth of n-type solar cells partly because of the challenge in achieving effective passivation of B emitter and the formation of boron-rich layer (BRL) during the diffusion.

Most current B diffusion processes used to fabricate n-type solar cell result in the formation of undesirable BRL which is located between the borosilicate glass (BSG) and $p^+$ region [6–9]. The BRL is known to act as high recombination site and may interfere with surface passivation [9–11]. It has been reported that the BRL can also cause degradation of bulk lifetime due to crystal defects resulting from the different thermal expansion coefficients between BRL and Si, which occurs during the cooling down [10,11]. Since both surface passivation and bulk lifetime are the key to high efficiency solar cells, BRL needs to be removed to attain high efficiency n-type solar cells. Thermal oxidation is often used to remove the BRL, but it causes degradation in bulk lifetime due to the injection of impurities from the BRL into bulk [9,12]. Kessler et. al. reported that carrier lifetime degradation can be avoided either by limiting the process temperature to 850 °C and thus preventing BRL formation or through reconverting the BRL by a drive-in step in oxidizing atmosphere [11]. Recently, we have shown that chemical etching treatment can effectively remove BRL without bulk lifetime degradation in the case of B emitter formed by screen printing paste and it can also improve passivation quality of implanted B emitter [9,13–15]. However, above reports have explored only the two extreme cases: (1) cells with full BRL intact and (2) cells with BRL completely removed. The impact of gradual etching of the BRL on cell performance has not been investigated systematically to provide a better understanding of the morphology, degradation mechanism, and impact of BRL thickness on cell efficiency. Thus, this paper talks about fundamental understanding, impact, and removal of BRL to attain well passivated high efficiency n-type Si solar cells.

In this paper, n-type PERT (passivated emitter, rear totally-diffused) solar cells were fabricated with controlled wet chemical etching of BRL to quantify the impact of partial and complete removal of the BRL on cell performance. In order to investigate the impact of impurities left in the partially etched BRL, a cell process

* Corresponding author.
*E-mail address:* yok6@mail.gatech.edu (Y.-W. Ok).

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was developed to partially etch the BRL first after the B diffusion followed by consumption of the remaining BRL by thermal oxidation to inject the remaining impurities in the BRL into the bulk. Detailed electrical and optical measurements, transmission electron microscopy (TEM), and auger electron spectroscopy (AES) measurement were performed to examine the morphology, thickness, and composition of the partially removed BRL and its impact on solar cell parameters.

## 2. Experiment

Large area (239 $cm^2$) n-type PERT solar cells were fabricated on 170 μm-thick and 5 Ω cm resistivity n-type Si wafers with the process sequence described in Fig. 1. Both surfaces of the wafers were randomly textured with upright pyramids followed by RCA cleaning. A liquid B paste was screen-printed on the entire front side followed by a drying step at a temperature of 200 °C. The samples were then annealed at a temperature of 1000 °C for 10 min to form a B emitter. After the B annealing, rear surface planarization was performed by protecting the front surface by PECVD silicon nitride ($SiN_x$) film followed by potassium hydroxide (KOH) etching for back planarization and subsequent removal of $SiN_x$ protective layer by hydrofluoric acid (HF) dip. Then the wafers received the chemical etching treatment [13] for different times ranging from 0 to 8 min. The mixture of HF, acetic acid ($CH_3COOH$), and nitric acid ($HNO_3$) (1:100:100) was used for the etching. Phosphorus (P) dopants were implanted on the entire rear side followed by 840 °C anneal/oxidation for 60 min to form $n^+$ back surface field. During the implant anneal, a thin thermal Si oxide layer (∼10 nm on front and ∼30 nm on back) was grown. This many not be enough to consume full BRL layer without etching. This oxidation step injects impurities contained in the remaining BRL into the bulk. Next, an appropriate thickness of PECVD $SiN_x$ layer was deposited on the front and back $SiO_2$ to serve as antireflective coating and effective passivation. The front grid pattern and point contacts on the back were screen-printed using Ag/Al and Ag paste, respectively, followed by a rapid co-firing step at ∼700 °C. Finally, a Ag reflector was printed on top of the rear screen-printed point contacts followed by a short low temperature (∼200 °C) drying step.

## 3. Results and discussions

Light *I–V* characteristics of the n-type PERT Si solar cells with different BRL etching time are summarized in Table 1. The open-circuit voltage ($V_{oc}$), short-circuit current density ($J_{sc}$), fill factor (FF), and efficiency ($\eta$) are plotted in Fig. 2 as a function of BRL etching time to gain a better understanding of the trend and impact of BRL thickness on cell parameter. Note that as the etching time increases, $J_{sc}$ increases linearly while $V_{oc}$ increases slowly up to an etching time of ∼4 min and after that the cell performance starts to decrease. The FF remains essentially unchanged until 4 min etching, and after that it decreases sharply. This behavior resulted in maximum cell efficiency at 4 min BRL etching time for the screen-printed B emitter used in this study.

Sharp drop in cell efficiency and FF beyond 4 min etching time can be explained by detailed series resistance ($R_s$) analysis using the methodology outline by D. L. Meier [16]. The TLM pattern analysis showed that contact resistance is very low until 6 min BRL etching time, but increased rapidly after 8 min etching time. It clearly shows that beyond 6 min etching, both sheet resistance and contact resistance start to increase $R_s$ because over-etching starts to reduce emitter surface concentration. The over-etching also showed an increase in the ideality factor $n$ from 1.06 to 1.14 which can be caused by junction leakage due to metal spiking when firing the screen-printed contacts through thinner emitter [17,18]. Finally, calculated FF values including the effect of $R_s$, $R_{shunt}$ and $n$-factor, are very consistent with the measured FF. (Table 2). In addition, emitter saturation current density underneath the metal contact region ($J_{0e,met}$) increases due to higher sheet resistance emitter, resulting in the decrease in $V_{oc}$ beyond 4 min

**Table 1**
Summary of light *I–V* results of n-type PERT solar cells with different etching times

| Etching time (min) | $V_{oc}$[mV] | $J_{sc}$[mA/cm$^2$] | FF [%] | $\eta$ [%] |
|---|---|---|---|---|
| 0 | 644 | 38.18 | 79.5 | 19.5 |
| 2 | 646 | 38.34 | 79.5 | 19.6 |
| 4 | 649 | 38.53 | 79.8 | 20.0 |
| 6 | 646 | 38.66 | 78.9 | 19.7 |
| 8 | 641 | 38.86 | 77.7 | 19.4 |

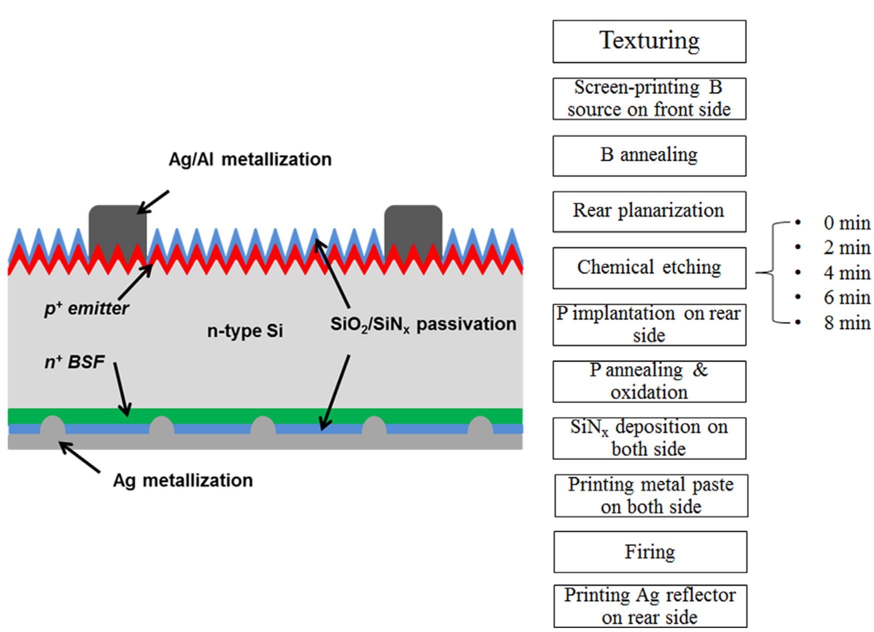


**Fig.1.** Schematic structure of n-type PERT (passivated emitter, rear totally-diffused) cell and the process flow.