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Influence of environmental temperature and device temperature difference on output parameters of c-Si solar cells

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ABSTRACT

Influence of environmental temperature and the temperature difference between the front and back surfaces of the cell on the output parameters of a typical commercial c-Si solar cell is analyzed by two-dimensional finite difference method. The results show that even for the cell with its front and back surfaces at the same temperature, the temperature distribution in the cell's interior is not homogeneous; the temperature difference between the front and back surfaces will generate a temperature gradient inside the cell; the temperature variation in the cell's interior for both the front and back surfaces at the same and different temperature can be divided into two regions; considering three heat mechanisms related with carrier transport process, Peltier and Thomson effects and Joule heat effects have more important influences on the temperature; with environmental temperature increasing, the values of open circuit voltage, fill factor and efficiency will all decrease and those of short current will increase; with the temperature difference increasing, the values of $|J_{sc}|$ and FF will decrease, but those of V_{oc} andη will increase.

1. Introduction

Crystalline silicon (c-Si) solar cells (SCs), which are the dominant products in the photovoltaic market, have been widely used to satisfy the electrical energy needs under various environmental conditions, including some extreme environmental conditions, such as high mountains, inhospitable deserts or islands in various latitudes. Due to the sensitivity of the c-Si material to environmental temperature, the output parameters of c-Si SCs will vary greatly in different environmental conditions. Therefore, the studies on the output parameters of c-Si SCs varying with temperature are very important for further extending their application ranges and predicting the output power of a photovoltaic (PV) system (Agarwala et al., 1980).

Researchers have paid much attention to investigating how the output parameters of c-Si SCs vary with temperature. The early results show that (Agarwala et al., 1980; Wysocki and Rappaport, 1960; Fan, 1986; Veissid et al., 1995) with the operating temperature of a c-Si SC increasing, the short current (J_{sc}) remains virtually unchanged and the open circuit voltage (V_{oc}), fill factor (FF) and efficiency (η) all decrease. During the past ten years, PV technologies have received heightened attention worldwide with the global PV installed capacity increasing substantially; the studies on the changes of the output parameters of c-Si SCs with temperature have gradually become a hot research area in the solar PV field. In 2003, Green has shown theoretically that the performances of c-Si SCs generally decrease with increasing temperature, fundamentally due to increased internal carrier recombination rates, caused by increased carrier concentrations (Green, 2003). In 2005, David et al. have studied both theoretically and experimentally that at a relatively high temperature (around 100–200 °C), the excessive heat in a PV system can be used to increase the total efficiency of solar energy utilization, taking account of the different carrier transport mechanisms and recombination parameters of the cell material (David et al., 2005). In 2008, Singh et al. have investigated that the rate of decrease of V_{oc} with temperature is controlled by the values of the band gap energy, shunt resistance and their rates of change with temperature (Singh et al., 2008). In 2012, Singh and Ravindra have further indicated that the reverse saturation current density has important effects on the efficiency of a c-Si SC varying with temperature (Singh and Ravindra, 2012). In 2014, Xiao et al. show that at high temperature, compensated c-Si SCs can generate more electricity than the conventional c-Si SCs, due to the lower temperature-variation of the minority electron mobility in compensated silicon (Xiao et al., 2014). In 2015, Ghani et al. have investigated that temperature affects each of the five characterization parameters required to characterize their electrical behavior by using the single diode five parameter model and obtained that the reverse saturation current is the most

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temperature sensitive characterization parameter (Ghani et al., 2015). These results show that the influence of temperature on the output parameters of c-Si SCs is related with the variations of the basic properties of c-Si materials with temperature.

Diode models are the most commonly used method to establish the relationships between environmental temperature and the output parameters of c-Si SCs (Agarwala et al., 1980; Fan, 1986; Green, 2003; David et al., 2005; Singh et al., 2008; Singh and Ravindra, 2012). For various diode models, there exists the same assumption that the temperature distribution is uniform, but in practical application, the temperature distribution of a c-Si SC will be inevitably influenced by environmental conditions, such as wind speed and solar radiation levels. Several researchers have indicated that a 1.5–3 K temperature difference (T_D) exists between the front and back surfaces (FBSs) of a c-Si SC during its normal operation process (Hosseini et al., 2011; Armstrong and Hurley, 2010; Indartono et al., 2015). In addition, three thermal mechanisms related to carrier transport process will also affect the temperature distribution of a c-Si SC. Therefore, diode model can only be considered as a good approximation to the actual operation situation of a c-Si SC.

Because many facts can affect the temperature distribution of a c-Si SC, its temperature distribution is essentially a spatial non-uniform temperature distribution. The spatial non-uniformity will pose a significant challenge in accurately testing the output parameters of a c-Si SC under different testing conditions, which usually specify that the temperature of the device under test (DUT) must be definite (for example the DUT is specified as 25 ± 1 °C under the Standard Testing Conditions (STC) of SCs). The exact simulation of the temperature distribution for a c-Si SC can help a lot to understand and correct the errors appearing in testing its output parameters under STC or other temperature conditions. In this paper, we will investigate the influences of the temperature non-uniformity on the output parameters of a typical commercial c-Si SC by solving Maxwell equations, stationary semiconductor device equations and heat flow equations by two-dimensional finite difference method. In our simulation, the temperature distributions and temperature gradients (T_gs) inside a c-Si solar cell are first obtained at the different temperatures and then the influences of these mechanisms on T_g values are further analyzed by comparing the heat released and absorbed by different thermal mechanisms. Finally the influences of T_g on the output parameters of the c-Si SC are discussed in detail.

2. Numerical method and cell structure

2.1. Numerical method

Two-dimensional finite difference method is used to solve Maxwell equations, stationary semiconductor device equations and heat flow equations, where the mesh technology are same in solving these equations. A detailed flowchart can be seen in Appendix. The finite difference frequency domain method is first used to solve Maxwell equations and obtain the steady-state distribution of optical intensity in the c-Si SC (Lu et al., 2013) and then the steady-state distribution of carrier-generation rate, which can be viewed as a constant charge source, is obtained by transforming the steady-state distribution of optical intensity (Chao et al., 2010). By introducing the charge source into the Poisson equation and temperature variable into the properties of c-Si material, the semiconductor device equations can be solved by enriched residual free bubble method proposed by Simpson et al. (2012). Finally, the temperature distribution of the c-Si SC and the heat absorbed and released by different mechanisms can be obtained by (https://en.wikipedia.org/wiki/Heat_equation)

$$C\frac{\partial T}{\partial t} = \nabla(\kappa\nabla T) + Q_{thermal} \tag{1}$$

where κ is the thermal conductivity, C is the heat capacity per unit volume and $Q_{thermal}$ denotes the heat generated per unit volume, which can be rewritten as (Ahmad and Gunther, 2004),

$$Q_{thermal} = \left(\frac{J_n^2}{qn\mu_n} + \frac{J_p^2}{qn\mu_p}\right) + \frac{R-G}{q}\cdot[(E_p - E_n) + T(P_n + P_p)] - \frac{T(J_n\nabla P_n - J_p\nabla P_p)}{q} \tag{2}$$

In Eqs. (1) and (2), the values of κ and C at different temperatures are from the website http://www.ioffe.ru/SVA/NSM/Semicond/Si/thermal.html and Glazov and Pashinkin (2001); q is unit charge; n and p denote the electron and hole concentrations, respectively; T is Kelvin temperature; J_n, J_p, μ_n and μ_p are the current densities and mobilities of electrons and holes, respectively; R and G are the carrier generation and recombination rates, respectively; E_n and E_p is the quasi-Fermi levels for electrons and holes, respectively; P_n and P_p are the thermoelectric powers for electron and hole, respectively. In Eq. (2), the first, second and third terms represent Joule heat (Q_J), heat absorbed or released in the generation and recombination process of carriers (Q_C) and heat generated by Peltier and Thomson effects (Q_{PT}), respectively.

In the finite difference method, the material properties and field parameters are defined at the different discrete grid points, in order to accurately resolve these properties and parameters, grid resolution, which is defined as the distance between a grid point and its neighbor, must be small enough, but excessively small resolution will increase greatly the computational burden. In general, the grid resolutions in c-Si SC simulations are often chosen to be on the order of $\lambda_{min}/40$ to $\lambda_{min}/10$, where λ_{min} denotes the minimum absorption wavelength of c-Si material.

2.2. Cell structure and its parameters

As shown in Fig. 1, a typical commercial c-Si SC structure mainly consists of Ag cathode, SiN_x anti-reflection coating (ARC), textured pyramid, c-Si active layer and Al anode on its back surface (Al BR). In Fig. 1, the thickness of c-Si active layer is denoted by $T + H$, where H is the height of pyramid; the layer thicknesses of Ag cathode, ARC and Al BR are denoted by $t1$, $t2$ and $t3$, respectively; the widths of periodically textured structure and Ag cathode are denoted by $w1$ and $w2$, respectively; the textured angle is denoted by θ. Here, we select that $H = 7$ μm, $T = 200$ μm, $t1 = 0.5$ μm, $t2 = 70$ nm, $t3 = 0.5$ μm, $w1 = 10$ μm, $w2 = 0.5$ μm and $\theta = 54.74°$, respectively. In this structure, ARC, periodically textured structure and Al BR form an effective light trapping structure.

In order to decrease the numerical errors arising from the finite-difference approximations, we adopt Yee grid resolution in both X and Y directions as one twentieth of the minimum absorption

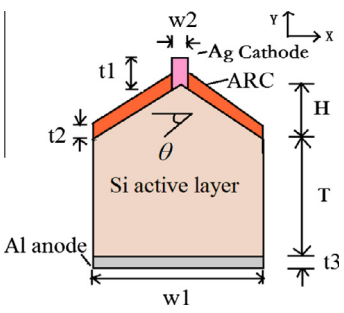

Fig. 1. A typical commercial c-Si SC structure.