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Low-energy ion implantation for shallow junction crystalline silicon solar cell

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Abstract

Ion implantation technique has been demonstrated to improve solar cell efficiency. In this study, we etched an as-implanted *p*-type wafer and then used an appropriate annealing condition to obtain an optimum surface doping profile for the emitter of a crystalline silicon solar cell. A SiO_2 layer was used both as a barrier layer for anti-outdiffusion and a surface passivation layer, which was deposited before the annealing process. An improvement in solar cell efficiency was demonstrated by low-energy phosphorus ion implantation at a proper dose.

Keywords: Ion implantation; Crystalline silicon solar cell; Implant energy

1. Introduction

Ion implantation technology has been widely used in silicon very-large-scale-integrated (VLSI) devices for shallow junctions (Plummer et al., 2001). In recent years, studies have revealed the advantages of ion implantation technology for solar cell fabrication (Boo et al., 2012; Choi et al., 2014; Hieslmair et al., 2012; Michel et al., 2015). Ion implantation can lead to low carrier recombination at the doped layer due to the formation of a shallow junction without forming silicate glass on the surface. With the single side doping technique, edge isolation step can also be dispensed. Compared with the conventional thermal diffusion method, implantation doping can manage to obtain more surface uniformity of dopant concentration.

During ion implantation, dopants are bombarded into the wafer and collide with silicon lattices. A cascade of defects are produced in the form of self-interstitial, implanted dopant impurities and vacancies. Dopant ions thus amorphize the silicon at the surface. Some silicon interstitials and vacancy defects begin to form a {3 1 1} plane during an annealing temperature at 400 °C, and the precipitates turn into dislocations loops at the end-of-range (EOR) region (Elliman and Williams, 2015; Mubarek, 2013; Tan et al., 2006). However, the amorphized layer can be recrystallized by solid phase epitaxial regrowth (SPER) (Noda et al., 2014; Olson and Roth, 1988; Puglisi et al., 2000; Ruffell et al., 2005b; Satta et al., 2006a,b; Suzuki et al., 2007a,b). This process can regrow amorphous silicon into a crystalline structure and induces a high concentration level at a temperature of 500–600 °C. However, a few point defects still remain after SPER annealing.

At a high dopant dose, the residual inactive dopants exist and contribute to secondary implantation damage. High temperature at a second annealing step is then required after the SPER process for the removal of the

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point defects. Nevertheless, it is tough to make a shallow junction at the second annealing step with a high temperature, because diffusion also occurs during dopant activation. Excess interstitials are deeply introduced into the crystalline silicon as the implanted dopants can diffuse much faster than expected. In fact, the diffusion time and annealing temperature dominate this transient enhanced diffusion (TED) effect (Chang et al., 2002; Chui et al., 2003; Simoen and Vanhellemont, 2009), which leads to the extent of dopants profile.

Thermal budget is the most important issue that should be concerned in conducting an annealing process. Annealing temperature dominates the density of secondary damage, controls the diffusion of dopant interstitials, and repairs the surface point defects. In this study, low energy phosphorus implantation for a doped p-type silicon wafer is carried out in order to understand the effect of the high temperature annealing on the dopant concentration profile and the resultant solar cell performance. Also, different implantation doses are considered in the process in which we add an etch step for as-implanted wafers and deposit a layer of silicon dioxide against outdiffusion as well as for surface passivation.

2. Experiments

Boron doped (1 0 0) oriented Czochralski-grown solar-grade silicon wafers were used in the experiments here. These wafers had thicknesses of 200 μm with resistivities of 1–3 Ω-cm. After texturing the wafers' surfaces by an alkaline solution, phosphorus $^{31}P^{+}$ was implanted into the substrates with a 7° tilt and 22° rotation to avoid channeling effect. The implantation energies were set at 10 keV, 30 keV, and 50 keV at doses of $5 \times 10^{15}\,cm^{-2}$, $3 \times 10^{15}\,cm^{-2}$, and $2 \times 10^{15}\,cm^{-2}$. The remaining ion contamination on the as-implanted surfaces were etched off by a diluted potassium hydroxide (KOH) solution and cleaned with SC2 solution followed by dipping in HF solution. The etching aimed to reduce surface recombination owing to the possible great amounts of inactive dopants. A 20 nm SiO_2 layer was then deposited on some of the samples by a plasma enhanced chemical vapor deposition (PECVD) machine. The other part of the samples had no such a layer for comparison. These wafers were loaded into a furnace at 550 °C for 10–30 min for elimination of {3 1 1} planes. Then, the furnace was ramped up at different temperatures from 780 °C to 900 °C for 30 min in a nitrogen ambient to achieve dopant activation. A SiN_x antireflection layer was coated on each front surface of the wafers. Silver paste and aluminum paste were screen printed on, respectively, the front and back sides of the wafers for metallization. Note that the size of each cell is $2 \times 2\,cm^2$, and that the front contact was in a grid pattern with a single busbar having a width of 1.5 mm in the middle, while the back contact was disposed over the whole surface of the back side. Finally, a co-firing process was performed in a door-shielded oven. To assure the uniformity of sheet resistance, samples were measured by the four point probe technique. Effective minority carrier lifetime prior to antireflection layer deposition was measured by quasi-steady-state photo-conductance (QSSPC) measurement. The doping concentration profile was analyzed using secondary ion mass spectrometry (SIMS). Implantation damage in the crystalline silicon was investigated by transmission electron microscopy (TEM). *I–V* curves of cells were measured under the standard condition at an intensity of 100 mW/cm^2 with an AM1.5G solar spectrum.

3. Results and discussions

3.1. Implantation damage

As pointed out by some researchers, nuclear stopping dominates the behavior of low-energy implanted ions colliding with silicon lattices (Paul, 2013; Plummer et al., 2001; Ziegler, 1999). Though, these low-energy implanted ions created damages to the crystalline structure of a silicon substrate. Here, we implanted some low-energy phosphorus ions into single-crystalline silicon substrates to demonstrate the damages, and see how much these damages can be cured by a thermal process. Bright field TEM images of as-implanted samples for 10 keV, 30 keV and 50 keV implant energies are shown in Fig. 1(a), (b) and (c), respectively. The dosage levels for these implant energies were $5 \times 10^{15}\,cm^{-2}$ (10 keV), $3 \times 10^{15}\,cm^{-2}$ (30 keV), and $2 \times 10^{15}\,cm^{-2}$ (50 keV). In Fig. 1(d), concentric circles of diffraction pattern show the amorphous structure near the silicon surface. Inside the silicon wafer, amorphous layer was forming along the projected range and expanded its depth as the implant energy increased. However, the amorphized Si layer would suppress ion channeling, though a large amount of defects were accumulated at the amorphous/crystalline (a/c) interface. Fig. 1(e) shows the TEM image of a wafer implanted at either 10 keV, 30 keV or 50 keV followed by an annealing process of 820 °C for 30 min. The diffraction pattern shown in Fig. 1(f) indicates the elimination of amorphous layer, which represents a good quality of crystalline structure as an emitter.

We have carried out a number of experiments with different implantation conditions, in which implant energy and implant dosage level were varied in forming an *n*+ emitter layer. We chose the implant energy 10 keV, 30 keV and 50 keV in this study, while the phosphorus dosage level were $2 \times 10^{15}\,cm^{-2}$, $3 \times 10^{15}\,cm^{-2}$ or $5 \times 10^{15}\,cm^{-2}$ for the aforementioned implant energies.

3.2. Recrystallization

We have carried out a two-stage annealing process to recrystallize the as-implanted wafers. In the two-stage annealing process, the as-implanted wafers were annealed first at 550 °C for 10, 20 and 30 min, respectively, and then the temperature was ramped up to a temperature over