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Dielectric barrier layers by low-temperature plasma-enhanced atomic layer deposition of silicon dioxide

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ABSTRACT

Electrothermal measurement techniques often require thin dielectric barriers to isolate active electrical test structures from samples of interest. The combined need for electrical passivation but thermal proximity necessitates the use of an electrically thick but thermally thin barrier layer. Here, we demonstrate a hybrid approach toward constructing sub-300 nm SiO_2 multilayer barriers based upon low-temperature plasma-enhanced atomic layer deposition and high density plasma chemical vapor deposition. Using pairs of buried metal test structures, we quantify changes in device resistance and cross-talk after covering the dielectric barrier with thin evaporated gold films and thick electroplated copper films. We show that a hybrid approach to passivating electrothermal measurement devices outperforms individual homogenous barriers formed by either deposition technique.

1. Introduction

Electrothermal measurement devices use metal thermal transducers (*i.e.* heaters) and metal thermal sensors (*i.e.* thermometers) to measure the thermal properties of bulk materials, thin films, and nanostructures [1–6]. Metal heaters generate Joule heating when driven with an electrical current, and metal thermometers use changes in electrical resistance to measure the associated temperature fields. These devices require well-controlled, isolated electrical pathways to accurately correlate the measured electrical signals to the thermal signals of interest. For dielectric samples and substrates, the heaters and thermometers can be in intimate contact with the sample material without electrical interference. However, when the samples are electrically conductive, such as semiconductors, metals, ionic solutions, and conductive polymers, the patterned test structures must be electrically-isolated from the sample. Thin film barrier layers are chosen for this role and are widely used to protect electronic devices from a variety of harsh operating conditions that include corrosive working fluids, oxidizing and reducing environments, and high electric fields.

Silicon is readily passivated through self-oxidation, but many other materials require the deposition of dielectric thin film barriers, ranging from high-*k* dielectrics (*e.g.* HfO_2 [7, 8]) to two-dimensional layered films (*e.g.* hexagonal boron nitride [9, 10]). Atomic layer deposition (ALD) is commonly used to deposit dense thin films for applications ranging from corrosion resistance of metals to dielectric barriers in microelectronic devices [11]. Furthermore, ALD can produce conformal films when depositing onto high aspect ratio device features [12]. For electrothermal devices, the barrier layer must satisfy two criteria: (1) be electrically thick to prevent both DC (resistive) and AC (capacitive, inductive) coupling contributing to signal loss, and (2) be thermally thin to preserve thermal measurement sensitivity to the material properties of interest. The first criterion is achieved by using a fully-densified, homogeneous, and pin-hole free dielectric film. The second criterion is achieved by minimizing the thermal resistance of this dielectric film by reducing the film thickness and/or by choosing a dielectric with sufficiently high thermal conductivity. In amorphous dielectrics frequently chosen for barrier applications, thermal conductivity scales with atomic density [13, 14]. For example, varying the deposition temperature of ALD processes has been shown to induce changes in Al_2O_3 film density by 15%, with a corresponding change in thermal conductivity of nearly 35% [15]. Such changes in SiO_2 films could reduce the thermal conductivity from 1.4 W/(m-K) at full density to 0.9 W/(m-K) and may impact the sensitivity of some electrothermal measurements. Therefore, both criteria benefit from increasing atomic density of barrier layers, a property often limited by the deposition method and process temperature (see Fig. 1) as well as post-deposition

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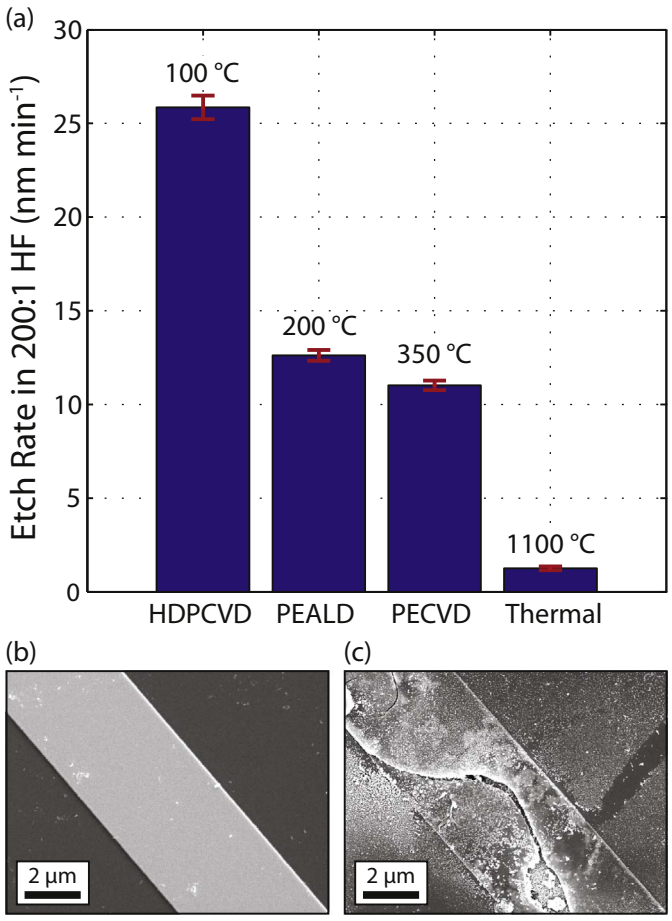

Fig. 1. (a) Wet etch rate of SiO_2 films in 200:1 HF grown by HDPCVD, PEALD, PECVD, and thermal oxidation in order of increasing deposition temperature. (b, c) Scanning electron microscopy images of a patterned metal line covered by a single layer of SiO_2 deposited by PEALD at an elevated temperature of 270 °C (b) as-fabricated and (c) after driving the device with a sinusoidal current to induce temperature oscillations.

treatments such as annealing.

In this article, we characterize the electrical isolation performance of high-quality silicon dioxide (SiO_2) multilayered barriers deposited using both low-temperature plasma-enhanced atomic layer deposition and high density plasma chemical vapor deposition processes. Silicon dioxide is an attractive barrier material due to its chemical inertness, optical transparency, and conventional integration with microfabrication. We assess the passivation characteristics using electrothermal test structures originally designed to measure thermophysical properties of nanostructured metal thin films [16, 17]. In brief, the test structures are fabricated onto a fused silica wafer using optical lithography, electron beam evaporation, and liftoff to pattern 5/60 nm of Ti/Pt into lines (1000 µm long, 5 µm wide) and are configured for four-point resistance measurements. The wafer is diced into chips that each contain two test structures separated by 1000 µm. The devices are then passivated using seven different combinations of processing, including plasma-enhanced atomic layer deposition (PEALD), high-density plasma chemical vapor deposition (HDPCVD), and post-deposition annealing. PEALD produces a high density SiO_2 film at a low deposition rate, whereas HDPCVD produces a lower density SiO_2 film but at a much higher deposition rate. PEALD of SiO_2 achieves density on the order of 2.07–2.12 g/cm^3 when deposited at comparatively low deposition temperatures of even 125 °C (*e.g.* [18]). Combined with its conformal properties, PEALD can achieve improved (lower) wet etch rates in dilute (200:1) HF as shown in Fig. 1 in comparison to the low temperature HDPCVD process, a characteristic associated with higher density, lower porosity, and lower impurity oxides.

While the intrinsic electrical resistivity only weakly depends on the film density, there is a much stronger correlation between film density and completeness of coverage. Low density films will include more pinholes and gaps in coverage than fully dense films. HDPCVD employs a high density plasma that both enables lower temperature deposition relative to PECVD and increases the etch component during deposition due to ion bombardment. The simultaneous deposition and etching create kinetic conditions ideal for gap filling that tends toward topology planarization and is not suited for conformal step-coverage (*e.g.* [19].). In contrast, PEALD of SiO_2 does not contain an etch component and relies upon self-limiting surface reactions that are ideally suited to provide conformal and pin-hole free coverage of high aspect ratio structures. In this work, the synergistic advantages of multimodal deposition are derived from the complementary capabilities of each technique, and we demonstrate that the multilayered barriers outperform the equivalent homogeneous layers of either PEALD or HDPCVD SiO_2.

2. Experimental details

All PEALD SiO_2 films are deposited at 200 °C in an Ultratech/Cambridge Nanotech Fiji hot-walled reactor using tris(dimethylamino) silane and a remote O_2 plasma. Depositions are performed using a continuous 130 sccm Ar carrier flow to promote precursor delivery and purging of reaction byproducts. The oxygen plasma is formed using 50 sccm O_2 and 300 W of inductively coupled plasma power. All HDPCVD SiO_2 films are deposited at 100 °C using a PlasmaTherm Versaline tool with an inductively coupled plasma (ICP) using silane and O_2 plasma [20]. An additional post-fabrication annealing at 600 °C for 6 mins in a 4% forming gas environment is used in some protocols to further densify the barrier layers and eliminate dangling bonds. All substrates were cleaned in an O_2 plasma immediately prior to barrier deposition by either method to remove surface organics and promote barrier adhesion.

Seven SiO_2 passivation configurations are examined in the present work, where each configuration is tested on eight test structures (four chips each containing two test structures). Set A contains only a single 215 nm-thick HDPCVD layer. Sets B through G begin with a 30 nm-thick PEALD layer to conformally coat the patterned metal features. A 215 nm-thick HDPCVD layer is added to Sets D through G to thicken the barrier. Sets F and G receive a final 30 nm-thick PEALD layer with the intention of covering any pinholes or other defects in the underlying

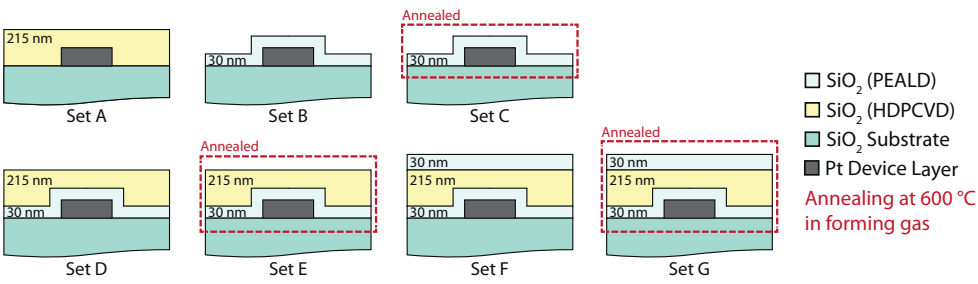

Fig. 2. Cross-sectional schematics (not to scale) of the seven different passivation layer combinations.