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Impacts of oxygen passivation on poly-crystalline germanium thin film transistor

Shoichi Kabuyanagi, Tomonori Nishimura, Kosuke Nagashio, Akira Toriumi

Department of Materials Engineering, The University of Tokyo, Bunkyo-ku, Tokyo 113-8656, Japan
Japan Science and Technology Agency (JST), CREST, Bunkyo-ku, Tokyo 113-8656, Japan

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ABSTRACT

We investigated the effects of the annealing ambient during solid phase crystallization (SPC) on the crystallization temperature of amorphous Ge and the electrical properties of a back-gated poly-crystalline germanium thin film transistor (poly-Ge TFT). Then, it was suggested that a slight amount of oxygen in Ge film and residual oxygen in the annealing ambient play important roles in Ge SPC. We found that the leakage current of poly-Ge TFT was well suppressed by performing SPC in N_2 or Ar which contains a slight but appreciable amount of residual oxygen, without decreasing the field effect mobility. In this paper, we discuss effects of the residual oxygen from the view point of defect passivation of Ge.

1. Introduction

Germanium (Ge) is considered to be a promising material to realize heterogeneous and three-dimensional integrated circuits [1] or "channel-last devices", because of its higher carrier mobility as well as its low processing temperature. In fact, solid phase crystallization (SPC) of amorphous Ge (*a*-Ge) has been achieved at a relatively low temperature (<500 °C) [2]. The high hole mobility of a polycrystalline Ge thin film transistor (poly-Ge TFT) on SiO_2, which exceeded the electron mobility of a poly-Si TFT fabricated by low-temperature SPC, was reported by Sadoh et al. [3]. However, the on/off ratio of poly-Ge TFTs ($\sim 10^2$) [3] was still much lower than that of the poly-Si ones ($\sim 10^8$) [4]. Therefore it is required to suppress the leakage current of poly-Ge TFTs. It is well known that point defects in Si films can be passivated by hydrogen, and that the on/off ratio and field effect mobility of the poly-Si TFT are improved [5]. In case of Ge, however, some groups have reported the positive effects of hydrogen passivation [6], but others have not [7]. In this study, we discuss the effects of the residual oxygen in the annealing ambient during SPC on the crystallization temperature of *a*-Ge and on electrical properties of back-gated poly-Ge TFTs. Then, several device parameters such as mobility, threshold voltage (V_{th}), and on/off ratio of poly-Ge TFTs are discussed from the view point of defect passivation by oxygen in poly-Ge.

2. Experimental procedure

n-Type Si substrates with thermally grown SiO_2 were prepared, and 25-nm-thick *a*-Ge films were deposited on SiO_2 at room temperature in ultra-high vacuum (UHV, the base-pressure was 5×10^{-8} Pa). SPC was carried out at 300–500 °C in UHV, H_2, N_2, or Ar ambient. Here, N_2 and Ar are regarded as the annealing ambient with the residual oxygen much more than UHV or H_2 ambient. In poly-Ge TFT fabrication, 500-nm-thick SiO_2 was formed on Ge film as the capping layer before SPC by using Spin-on-Glass, which suppressed the roughening of the poly-Ge surface during SPC. After removing the capping layer with a diluted HF solution, Ge islands were defined by wet etching with $H_2O_2 + H_2O$ solution, and Al was deposited and patterned for source/drain on Ge islands. Al was also deposited on the backside of Si as the back gate electrode.

3. Results and discussion

3.1. Crystallization temperature of a-Ge

The surface morphology of Ge film after SPC annealing was observed by an atomic force microscope (AFM) (SII, SPI4000) operated in dynamic mode with a cantilever, as shown in Fig. 1. The surface roughness of Ge film annealed at 300 °C in UHV is much larger than annealed in N_2, indicating that *a*-Ge crystallizes around 300 °C in UHV while it does not in N_2. Fig. 2 shows Raman spectra of Ge films after annealing in UHV and N_2 ambient. Here, a Raman Spectroscopy System (Horiba, LabRAM HR-800) with Ar laser ($\lambda = 488$ nm) was used. It is clearly observed that *a*-Ge film crystallizes at lower temperature by UHV annealing (UHV-A) than by the N_2 one (N_2-A). The crystallization temperatures (T_C) in

E-mail address: kabuyanagi@adam.t.u-tokyo.ac.jp (S. Kabuyanagi).

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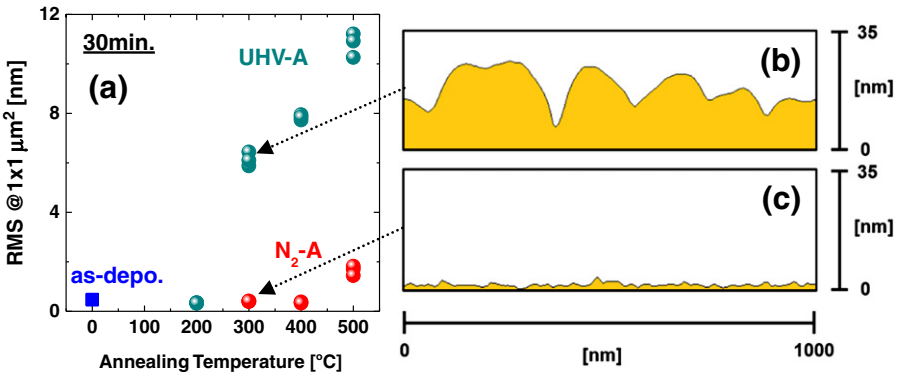

Fig. 1. (a) RMS surface roughness of Ge films on SiO_2 before/after annealing in UHV and N_2 for 30 min at 300–500 °C. (b, c) AFM images of raw profiles after annealing at 300 °C in (b) UHV and (c) N_2. All of the Ge films are deposited in UHV at room temperature, and the initial thickness of Ge film is 25 nm.

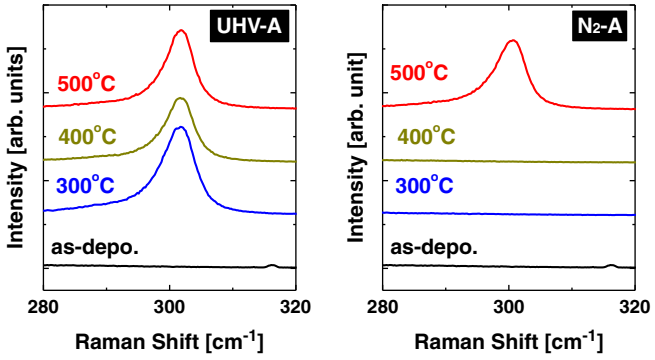

Fig. 2. Raman spectra of Ge films on SiO_2 before/after annealing at 300–500 °C in UHV and N_2 for 30 min. The deposition condition of Ge films is the same as Fig. 1.

various ambients reported by other groups are summarized in Table 1. The annealing time which is needed to fully crystallize *a*-Ge films at each T_C is also represented. These results are consistent with the present ones.

The difference of T_C of *a*-Ge between N_2-A and UHV-A suggests that Tc depends on the oxygen partial pressure of ambient during SPC. The phenomenon seems to be similar to the desorption reaction of GeO triggered by the reaction at GeO_2/Ge interface [14]. On the other hand, we confirmed that as-deposited Ge film contains oxygen atoms in the range of 10^{19}–10^{21}/cm^3 by SIMS, and the GeO desorption from an *a*-Ge/SiO_2/Si stack occurred around 300 °C by TDS (data is not shown). Therefore, it is inferred that the GeO desorption from *a*-Ge film may occur during SPC and make it easier to crystallize *a*-Ge in UHV where the oxygen partial pressure is lower, like the Vo mediated crystallization of GeO_2 reported by Wang et al. [15]. Thus, it is suggested that oxygen in Ge film and residual oxygen in annealing ambient play important roles in Ge SPC.

Table 1
The crystallization temperatures (T_C) in various ambients reported by other groups. The annealing times which are needed to fully crystallize *a*-Ge films at each T_C are also represented.

Reference	[8]	[9]	[10]	[11]	[12]	[13]
Ambient	N_2	He	N_2	N_2	Vacuum	Vacuum
T_C	470 °C	425 °C	410 °C	400 °C	390 °C	375 °C
Annealing time	3 h	25 h	25 h	20 h	1 h	10 min

3.2. Electrical properties of poly-Ge TFT

In poly-Ge TFT fabrication, SPC was performed by the two-step annealing method proposed by Toko et al. [2]. According to their report, the 1st SPC (425 °C, 8 h) determines the grain size of poly-Ge and the following 2nd SPC (500 °C, 2 h) decreases the defect density of each grain, as schematically described in Fig. 3. It means that effects of ambient during the 2nd SPC on properties of poly-Ge can be investigated by performing the 1st SPC in the same condition. Fig. 4 shows transfer characteristics of poly-Ge TFTs, where the 1st SPC was conducted in UHV, followed by the 2nd SPC in UHV, H_2, N_2 or Ar ambient. The electrical properties were measured by using the semiconductor device parameter analyzer (Agilent, B1500A). We can clearly observe that the ambient during the 2nd SPC affects the threshold voltage and on/off ratio of poly-Ge TFTs. On the other hand, the field effect mobility does not change significantly. On/off ratio of ~10^3 was obtained by N_2-A which was higher than the reported value [3].

Fig. 5 summarizes the off-current of poly-Ge TFT as a function of the threshold voltage. Then, it is found, in case that Ge SPC is performed in the ambient which contains the larger amount of residual oxygen, that both the threshold voltage and the leakage current decrease. As mentioned above, the grain size of poly-Ge was almost fixed by the 1st SPC, so that we can consider that the decrease of the leakage current is not caused by the change of grain size.

Threshold voltage (V_{th}) of the accumulation-mode device can be described by

$$V_{th} = \phi_{MS} + \phi_F + \frac{Q_i}{C_{OX}} + \frac{qN_A}{C_{OX}} T_{Ge}, \quad (1)$$

where ϕ_{MS} is the gate-channel work function difference, ϕ_F is the equilibrium Fermi potential, Q_i is the charge density at the interface states, C_{OX} is the oxide capacitance, q is the electronic charge, N_A is acceptor doping density and T_{Ge} is the thickness of poly-Ge film [16]. Here, V_{th} is defined as the gate voltage when the Ge channel is fully depleted.

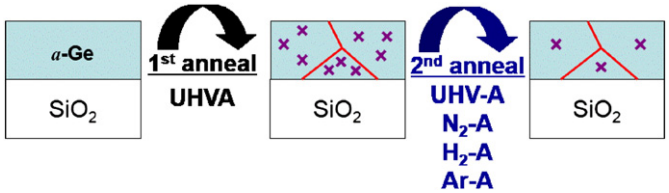

Fig. 3. Schematics of two-step annealing method where the 1st SPC was conducted in UHV, followed by the 2nd SPC in UHV, H_2, N_2 or Ar ambient. To investigate the effects of SPC ambient, grain size of poly-Ge was fixed by performing the 1st SPC in the same condition.