Journal of Manufacturing Processes 32 (2018) 222–229

Contents lists available at ScienceDirect

Journal of Manufacturing Processes

journal homepage: www.elsevier.com/locate/manpro

Technical Paper

Multilevel process on large area wafers for nanoscale devices

B.J. Pires[a,1], A.V. Silva[a,b], A. Moskaltsova[a,2], F.L. Deepak[c], P. Brogueira[b,d], D.C. Leitao[a,b,*], S. Cardoso[a,b]

[a] INESC – Microsystems and Nanotechnologies (INESC-MN) and IN, Rua Alves Redol 9, 1000-029 Lisboa, Portugal
[b] Instituto Superior Tecnico (IST), Universidade de Lisboa, Av. Rovisco Pais, 1049-001 Lisboa, Portugal
[c] Department of Advanced Electron Microscopy, Imaging and Spectroscopy, International Iberian Nanotechnology Laboratory (INL), Av. Mestre Jose Veiga, Braga 4715-330, Portugal
[d] CeFEMA, Instituto Superior Tecnico (IST), Universidade de Lisboa, Av. Rovisco Pais, 1049-001 Lisboa, Portugal

ARTICLE INFO

Article history:
Received 11 September 2017
Received in revised form 25 January 2018
Accepted 26 January 2018

Keywords:
Nanofabrication
Electron beam lithography
Reactive ion etching
Metrology

ABSTRACT

Spintronic nanodevices are consolidating a highly reputed position in advanced manufacturing industry, not only due to progresses in magnetic hard disk sensors, but also the memory market. The ability to integrate magnetic thin films on large area wafers and subsequent nanofabrication into functional devices is key for such success. This work describes methodologies used for definition of sub-100 nm pillars, using reliable via opening to contact nanopillars buried in a dielectric film. A two consecutive step electron beam lithography process is used to fabricate current-perpendicular-to plane nanodevices. The first step is required to pattern nanopillars down to 30 nm. The second provides access to nanopillar top through nanovias definition and reactive ion etching. Optimum alignment of multilevel exposures ensures the most accurate positioning in the shortest time. Most importantly, the results are obtained on 150 mm diameter wafers, where additional challenges of uniformity of resists, oxides and metals are critical for end-point control and improved yield of fabricated devices. The design of customized test structures allowed control of etching end-point.

1. Introduction

The semiconductor industry drives the metrology settings and nanofabrication standards in electronic device manufacturing. Given the reality of globalized markets, the massive production nodes of the semiconductor industry offer advanced manufacturing capabilities for other technologies, seeking a nanoelectronic capability extension [1,2]. One such example is spintronics, where the semiconductor industry could offer additional electronic functionalities, enabling nanofabrication of monolithic devices (e.g. MRAM, oscillators or read heads) by using compatible processing tools. Therefore an explosive growth in production capability for such devices requires manufacturing over large area wafers with large yield of functional structures. As industry maintains a high degree of confidentiality, the challenges in integrating and matching nanofabrication processes at distinct patterning levels is mostly overlooked in literature. Research groups working on spintronics have been consolidating advanced deposition, nanopatterning and metrology [3,4], compatible with large area wafers [5–7]. Although few reports exist on successful processes carried out by industry [7–9], many technical achievements remain not available in scientific publications.

Two of the challenging points across the spintronic nanodevice fabrication in 150 mm wafers are definition of sub 100 nm pillars and nanovia access to them. Lift-off has been employed in 25 mm substrates achieving magnetic tunnel junctions (MTJ) $\geqslant$100 nm [10]. Chemical mechanical polishing (CMP) reduces process time (compared to liftoff) [11,12,5] but requires a tight control of the end-point. Ion beam dry planarization has also been used [13], as do self-aligned methods although requiring careful matching between photoresist thickness and oxide etching rates, together with a controlled reactive ion etching (RIE) uniformity [14]. A broad view of the challenges and strategies used for magnetic device nanopatterning can be found in reference [3].

The strategy described here includes a two-step electron beam lithography (EBL), combined with nanovia opening using RIE. The alignment of multilevel features using optical lithography and EBL is optimized to ensure the most accurate positioning in the short-

* Corresponding author at: INESC – Microsystems and Nanotechnologies (INESC-MN) and IN, Rua Alves Redol 9, 1000-029 Lisboa, Portugal.
[1] Presently at International Iberian Nanotechnology Laboratory (INL), Av. Mestre Jose Veiga, Braga 4715-330, Portugal.
[2] Presently at Center for Spinelectronic Materials and Devices, Department of Physics, Bielefeld University, Universitätsstraße 25, 33615 Bielefeld, Germany.

https://doi.org/10.1016/j.jmapro.2018.01.024
1526-6125/

est exposure time. Furthermore, this study is performed in large area wafers where additional challenges regarding uniformity of resist layers, oxide films and metallic thin films, over the whole surface area, are critical for an improved yield of fabricated devices. These methodologies are somehow followed by the semiconductor industry, however the particularity of spintronic devices laid on ultrathin films (e.g. 1 nm critical thickness for the MTJ tunnel barrier, thin dielectric layers, thin resist thickness), imposes very narrow tolerances for the etching end-point control. The inclusion of customized test structures allowed to control the RIE end-point. As a result, we demonstrate a controlled nanofabrication process that can be followed in pre-production stages, shortening the path from innovative spintronic materials and devices to a large scale manufacturing level in a semiconductor-compatible foundry facility.

2. Results and discussion

Fig. 1 illustrates the main fabrication steps. The optimization of the proposed nano-process includes: (i) exposure of the nanovias by EBL critically aligned over nanopillar buried in oxide and (ii) accurate control of the RIE end-point for opening vias. Monitoring of deposition and etching uniformity during this step is key for a successful nanofabrication over the whole wafer area.

One starts by the deposition of the magnetic tunnel junction (MTJ) stack on a Nordiko 3000 ion beam deposition (IBD) tool. The used stack was based on the following structure: buffer/CoFeB/AlOx/CoFeB/cap, where the oxide barrier is 14 Åthick. The barrier oxidation was performed with remote plasma oxidation with a mixed Ar-O_2 plasma for 15 s after each 7 Å deposition of Al (pressure 0.6 mTorr, plasma voltage ≈15 V) [15]. A thick cap, usually Ta, is required as protective layer during RIE via opening. Ta provides a low etching rate and low material cost (compared with Pt, a highly selective alternative).

Bottom electrode (BE) is defined using optical lithography and Ar^+ ion milling at 70° (beam current 105 mA, ≈390 μA/cm^2 with +735 V; working pressure of 0.2 mTorr) [Fig. 1(B)].

2.1. Nanopillar definition

The wafer is then spin-coated with an electron sensitive negative resist whose thickness is critical to achieve EBL minimum size in the used tool (≈30 nm) [12]. A systematic study of spinning time, velocity, dispensed volume, and their impact on thickness (t_{avg}) and (non)uniformity (NU_{res}) was performed. Fig. 2(a) and (b) shows a representative t_{res} wafer map, from which we extract NU_{res}, calculated as $\frac{t_{max}-t_{min}}{2t_{avg}}$. Average resist thickness (t_{avg}) is calculated from 72 points uniformly distributed over the wafer, and its dependence on the spinning speed is depicted in Fig. 2(c). A decrease of t_{avg} to (87.0 ± 0.5) nm and NU_{res} to 1.1%, was obtained with increasing spinning speed up to 4 krpm. For spinning durations larger than 30 s, no significant uniformity improvement was observed. The optimized recipe was then used (spinning speed = 4 krpm during 30 s) followed by a bake at 85 °C for 60 s.

EBL is performed on a Raith-150 system using an acceleration voltage of 20 kV and aperture size of 10 μm, corresponding to beam currents ≈33 pA. Circular pillars were defined using the dot exposure mode. Fig. 3 displays the calibration curve for dot size versus dose, showing a linear dependence below 100 nm. For process validation a dot dose of 0.045 pC was used for a nominal dot diameter of 70 nm. The beam focal distance was controlled and corrected via software, to ensure well defined nanostructures along the entire wafer with size deviation from nominal of the order of 5%. This strategy showed an improvement on pillar maximum resolution

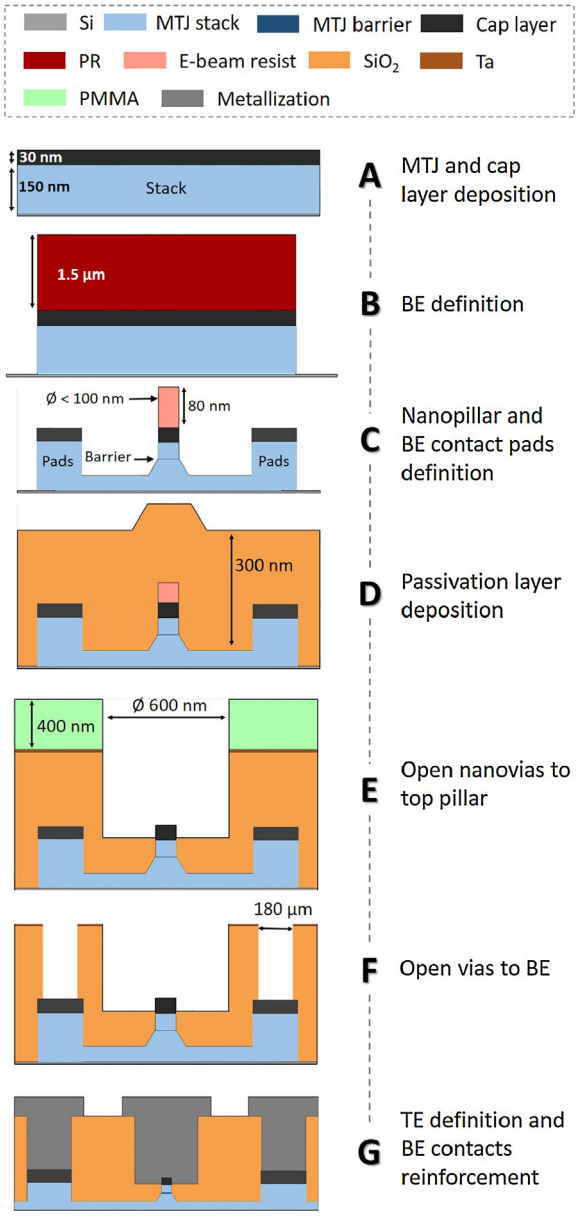

Fig. 1. Layout of the nanofabrication process: (A) MTJ and cap layer deposition, (B) BE definition by optical lithography and ion beam etching, (C) nanopillar and BE contact pads definition by EBL and two-step ion beam etching, (D) passivation layer deposition, (E) opening of the nanovias to top pillar contact, (F) opening of the vias to bottom pads using RIE and (G) TE definition and BE contact pads reinforcement by optical lithography and metallization. Schematics not to scale.

compared to area mode exposure, but with a strong dependence on stigmation correction and aperture alignment.

For long exposures, the stage drift relative to electron beam fixed position has also to be taken into account. According to Goodberlet et al., thermal effects and/or charging may be at the origin of the observed drift over time [16]. In this case, an incremental deviation will affect precision alignments such as via-to-pillar. Quantification was performed by scanning a cross-shaped mark every minute (up to 7h) and measuring its deviation relative to the center [Fig. 4(a)–(c)]. Fig. 4(d) shows all measurements overtime for both x and y directions. A plateau is visible over the first minutes upon loading the sample, starting to increase after ≈150 min. This difference is attributed to thermalization of the column and sample [16], and is consistent with information from manufacturer. Overall, a drift smaller than 3.5 nm/min is observed. Although for short