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Design of Barrier Bucket Kicker Control System

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Abstract

The Heavy-Ion Research Facility in Lanzhou (HIRFL) contains two synchrotrons: the main cooler storage ring (CSRm) and the experimental cooler storage ring (CSRe). Beams are extracted from CSRm, and injected into CSRe. To apply the Barrier Bucket (BB) method on the CSRe beam accumulation, a new BB technology based kicker control system was designed and implemented. The controller of the system is implemented using an Advanced Reduced Instruction Set Computer (RISC) Machine (ARM) chip and a field-programmable gate array (FPGA) chip. Within the architecture, ARM is responsible for data presetting and floating number arithmetic processing. The FPGA computes the RF phase point of the two rings and offers more accurate control of the time delay. An online preliminary experiment on HIRFL was also designed to verify the functionalities of the control system. The result shows that the reference trigger point of two different sinusoidal RF signals for an arbitrary phase point was acquired with a matched phase error below 1° (approximately 2.1 ns), and the step delay time better than 2 ns were realised.

Key words: Barrier bucket; Kicker; FPGA; ARM; Phase matching

1. Introduction

The barrier bucket (BB) method was proposed in 1983 by J.E. Griffin at Fermilab [1]. The concept is based on the application of a periodic radiofrequency (RF) voltage pulse synchronised with the revolution frequency of particles in a cyclic accelerator for storage and/or acceleration of charged particles [2]. By using this method, multiple injections and beam accumulation can be achieved through the

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