Nuclear Instruments and Methods in Physics Research A 731 (2013) 229–233

Contents lists available at ScienceDirect

Nuclear Instruments and Methods in Physics Research A

journal homepage: www.elsevier.com/locate/nima

Evaluation of data-acquisition front ends for handling high-bandwidth data from X-ray 2D detectors: A feasibility study

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ARTICLE INFO

Available online 14 May 2013

Keywords:
Synchrotron radiation instrumentation
Data acquisition system
X-ray imaging
FPGA
FMC

ABSTRACT

Two-dimensional (2D) X-ray detectors are indispensable for synchrotron radiation and X-ray free-electron laser experiments, such as coherent X-ray imaging, spectroscopy, and time-resolved experiments. In these experiments, special, temporal, or photon-energy information is projected onto the surface of a 2D X-ray detector, and it is generally accepted that detectors with a larger number of pixels and a higher dynamic range will provide better information on the sample. An example of a high-performance application in this area is SOPHIAS (Silicon-On-Insulator Photon Imaging Array Sensor), which is a next generation detector under development at the SPring-8 facility, Japan. Since such systems demand a high-bandwidth front end for data acquisition (DAQ), a prototype front end for SOPHIAS is also under development. Here, we have performed a feasibility study of the prototype front end using an evaluation board, which consists of an FPGA (field-programmable gate array) with an FMC (FPGA mezzanine card) interface to support various physical layers of sensor readout modules and back-end DAQ. The bandwidths were measured for various combinations of protocols and physical layers. In many photon science applications, scalability from a single module to many modules is important, so a compact desktop-type DAQ system was also evaluated. Measurements of the bandwidth using the evaluation board indicated that an effective bandwidth of 9 Gbps and 16 Gbps was achieved using SFP+ (Small Form-factor Pluggable Plus) with XAUI (X (ten) Attached Unit Interface) and PCI Express (Peripheral Component Interconnect Express), respectively.

1. Introduction

SACLA (SPring-8 Angstrom Compact free electron Laser) is an X-ray free-electron laser (XFEL) facility, which is part of the SPring-8 (Super Photon Ring-8 GeV) facility, and is capable of producing high peak brilliances and femtosecond-order X-ray pulses [1,2]. For coherent X-ray experiments using SACLA, a novel detector was required, and therefore, the new pixel array sensor, MPCCD (multi-port Charge-coupled device), has been developed at SPring-8. The detector is composed of eight tiled MPCCD sensors, allowing a larger imaging area to be covered [3], and a successful data acquisition (DAQ) system for the MPCCD detector is in operation [4].

A next-generation sensor, the Silicon-On-Insulator Photon Imaging Array Sensor (SOPHIAS) [5], is under development. The pixel structure of SOPHIAS is based on Silicon-On-Insulator (SOI) multi-via concept. Each implant region is connected to the readout circuit by metal via. By adjusting the number of via connections, biased charge collection is possible. This structure enables a wider dynamic range to be achieved. The front-end readout system acquires analog signals from the sensor, and applies an analog-to-digital signal conversion. This system can apply simple on-the-fly data conversion that can align the acquired digital signal allowing proper data transmission protocols, and the bandwidth of SOPHIAS will eventually exceed 10 Gbps. Table 1 compares the specifications of the detectors and DAQ systems for MPCCD and SOPHIAS. Since the current DAQ system cannot satisfy the bandwidth requirement of the SOPHIAS detector, a next-generation DAQ system that can handle bandwidths above 10 Gbps is required. The design of the SOPHIAS detector consists of 40 tiled sensors, and therefore, the new DAQ system will be a large-scale network-distributed system in which a large number of front-end and back-end systems will be connected by network switches. It is planned that SOPHIAS will be upgraded in phases, and its interface will be changed based on the required bandwidth performance for the given phase. In SACLA, one beamline is currently in operation, but eventually five beamlines will be operated.

The SPring-8 site also has another synchrotron radiation facility, SPring-8, which is a large 8-GeV storage ring accelerator complex with beamlines for synchrotron radiation experiments.

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http://dx.doi.org/10.1016/j.nima.2013.05.019

Table 1
Sensor and data acquisition specifications. The specifications of the SOPHIAS detector and associated front-end DAQ system are still under consideration, and thus ranges of possible values are given and some values are still to be decided (TBD). "CL base" means Camera Link base configuration: an interface standard for imaging data communication.

	MPCCD	SOPHIAS
Single sensor spec		
# of pixel	0.53 M	~2 M
Depth (bit)	16	16~32
Frame rate (Hz)	60	60~300
Throughput (Gbps)	0.5	2~20
FE DAQ spec		
Input (Gbps)	<2.04 (CL base)	TBD
Output (Gbps)	<1 (GigE)	TBD

There are around 60 beamlines for mid-scale experimental systems composed of only a few sensors and one desktop-type DAQ system. The SPring-8 site thus has both XFEL and synchrotron radiation facilities on one site, and both larger-scale high-bandwidth network-distributed DAQ systems, as well as smaller-scale DAQ systems, are required for the various types of experiments conducted here. Therefore, we have developed a new front end DAQ system with high bandwidth capabilities, but which can also be used for general purposes. The new front end DAQ must be able to handle bandwidths above 10 Gbps and support various scales of experimental systems composed of sensors, computing systems, and storage systems. Since new interfaces and standards must be supported within a short time period and also satisfy future requirements of the synchrotron radiation experiments, the system has been primarily developed using commercial off-the-shelf (COTS) components.

2. Evaluation System for prototype front-end DAQ system

As described in Section 1, one of our target applications is SOPHIAS, and the new DAQ system will be developed and upgraded along with each phase of the development of SOPHIAS. The new DAQ system will be a network-distributed system, but we will also consider more compact DAQ systems, such as a desktop-scale system.

First, we designed the concept of the new DAQ system, and then appropriate front-end DAQ system components were selected to satisfy the design requirements. Based on this design, we have developed a prototype front-end DAQ system and an Evaluation System to test its performance.

2.1. Design of new DAQ system

The front-end DAQ system for 2D pixel imaging sensors in SPring-8 must be able to support various input/output interfaces with high-bandwidth data transmission. Fig. 1 shows the conceptual design of the new DAQ system for a single sensor, in which high-bandwidth output data from the sensor is transmitted to a front-end DAQ system.

The front-end DAQ system will employ a metal or an optical cable as the physical interface for the input data. If data transmission over long distances or electrical isolation between the sensor and front-end DAQ system is required, optical cables will be used. We have considered several kinds of transmission data protocols and special protocols for imaging data, some of which have simple structures that can easily be applied to high-bandwidth data. However, some imaging protocols (e.g., Camera Link) used for cameras have complicated structures and can cope with only relatively low bandwidths.

After data has been transmitted from the sensor to the front-end DAQ, it must be transformed to an appropriate data structure suitable for the computing platform. Additionally, data buffering is important to account for differences between the data transmission schemes of the sensor and computing platform. The interface with the computing platform depends on the scale of the entire DAQ system. In the case of network-distributed systems, Gigabit-Ethernet will be adopted to connect many networked components. In the case of smaller-scale experiments, only a single desktop-sized PC will be needed to capture and store sensor data. Therefore the front-end DAQ system must be able to support various interfaces and to be modified to the scale of the particular system.

2.2. Hardware components

Hardware components for the front-end DAQ system were selected to support variety of interfaces with high-bandwidth data transmission. The requirements and associated technologies are as follows:

- High-bandwidth data transmission
  An FPGA (Field Programmable Gate Array) with multi-gigabit-transceivers was selected. The number of transceivers and the bandwidth must be sufficient to support both input and output interfaces.
- Support of various input/output interfaces
  An FMC (FPGA mezzanine card) [6] was selected. It delivers high-bandwidth performance of 10 Gbps per individual signal and 40 Gbps with a carrier card. To support both the input and output interfaces of our experiments, at least two FMC connectors are necessary. The FMC standard has two configurations depending on the number of standard I/O and multi gigabit transceiver connections; HPC (high pin count) [6] with 400 I/Os including more than eight transceivers was selected. The interfaces provided by the FMC can be reused if we change the carrier board in the future.
- Direct connection to computing platform
  This depends on the motherboard interfaces of the computing platform. Recently, the PCI Express (Peripheral Component Interconnect Express) [7] interface has become generally available on PCs, and there are various possible configurations depending on the signal-lane bandwidth and number of lanes.

A PCI Express board appropriate to the motherboard with an FPGA and FMC was adopted for our feasibility study. Table 2 shows the specifications of the evaluation board. The selected FPGA has 24 transceivers each with a maximum bandwidth of 6.5 Gbps. These transceivers are connected to the PCI Express (eight transceivers) and two FMCs (eight transceivers each).

The input/output interfaces of three FMC cards were prepared and evaluated to examine the effects of two physical layers and two transmission protocols, and the results are shown in Table 3. Thus, by swapping between these FMC cards, the various physical layers and protocols could be studied using only one pair of FPGA evaluation boards.

2.3. Data transmission protocols and physical layers

In this study, AURORA [8] and XAUI (X (ten) Attached Unit Interface) [9] were selected as the data transmission protocol. AURORA is a simple serial transmission protocol, and therefore easier to implement than other protocols. It has a lane-bonding function that bundles several AURORA channels as one broadband transmission. Since the selected FPGA has 6.5 Gbps multi-gigabit-