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Method Article

Beam position monitor gate functionality implementation and applications

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A B S T R A C T

We introduce a novel technique to implement gate functionality for the beam position monitors (BPM) at the National Synchrotron Light Source II (NSLS-II). The functionality, now implemented in FPGA, allows us to acquire two separated bunch-trains' synchronized turn-by-turn (TBT) data simultaneously with the NSLS-II in-house developed BPM system. The gated position resolution is improved about 3 times by narrowing the sampling width. Experimentally we demonstrated that the machine lattice could be transparently characterized with the gated TBT data of a short diagnostic bunch-train Cheng et al., 2017; Li et al., 2017. Other applications, for example, precisely characterizing storage ring impedance/wake-field through recording the beam positions of two separated bunch trains has been experimentally demonstrated.

- *Gated BPM signal processing improves the position resolution.*
- *Transparent lattice measurement using the gate function with diagnostic bunches.*
- *Collective effect study with simultaneous position measurement from two gates.*

A R T I C L E I N F O
Method name: Gated signal processing
Keywords: BPM, Signal processing, Gate, Lattice, Impedance, Closed orbit
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Specifications Table

Subject area	• *Physics and Astronomy*
More specific subject area	*Particle accelerator physics*
Method name	*Gated signal processing*
Name and reference of original method	*NSLS-II BPM electronics*
Resource availability	

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Method details

Introduction

The NSLS-II in-house developed BPM [3–5] adopts bandpass sampling theorem [6] for precise beam position measurement, similar to other modern BPM electronics. The BPM provides various beam position data acquisition for the routine operation and machine studies. Raw analog-to-digital (ADC) data is typically used for single pass (or first turn) measurement and BPM timing alignment; turn-by-turn (TBT) data processed from 310 ADC samples (for the NSLS-II storage ring) is widely used for physics studies; ~10 kHz fast acquisition (FA) data, further decimated from TBT data, is used for fast orbit feedback and active interlock for machine protection; 10 Hz slow acquisition (SA) data is typically used for closed orbit measurement and is streaming out through control network. FA data is well suited to study the performance of orbit stability within the range of 1 Hz to ~kHz. FA data is shared around the ring through cell controllers and serial data interface (SDI) fiber link with low latency.

In storage rings, the beam-induced signal on the button BPM contains harmonics of the bunch revolution frequency (RF frequency if all buckets are evenly filled). BPM electronics typically works at one of these harmonics below the chamber cutoff frequency, to eliminate possible high-order mode signals. The button signal has a pulse width of ~100 ps, which depends on bunch length, button capacitance, and cable attenuation. A low pass filter is used to remove the high-frequency components of the button signal. Similar to many other light sources, the NSLS-II ring has RF frequency at 500 MHz, the BPM electronics was designed to detect the button signal at the 1st harmonic of RF frequency. As illustrated in Fig. 1, which includes major components of BPM system before the digitizer, a bandpass filter (BPF) has ±10 MHz bandwidth with a center frequency of 500 MHz. The BPF broadens BPM button signal to ~200 ns. Amplifiers and attenuators are added to further condition beam signals to a large dynamic range for various beam currents and filling patterns. A 16-bit ADC digitizes the signal for digital signal processing, 310 times per revolution period. Typical fill pattern during operation has ~80% buckets filled out of 1320, therefore the majority of the ADC samples in one turn includes beam position information. However, during machine development or studies, the beam is typically filled with a short bunch train or single bunch. In this case, the beam-induced signal appears on a small fraction of 310 ADC samples in one turn, as shown in Fig. 1 which plots the ADC data with two bunch

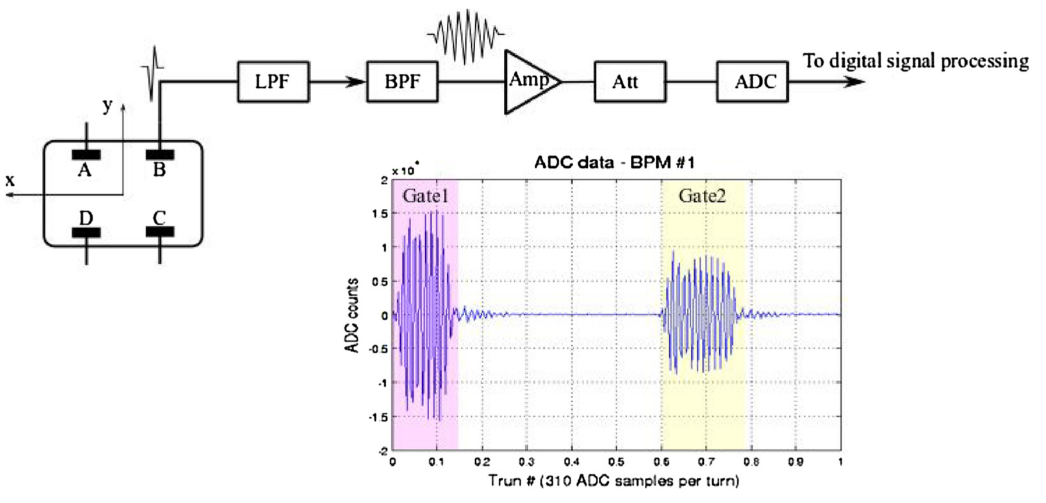

Fig. 1. Schematic diagram of major analog signal conditioning blocks for the NSLS-II BPM electronics. The embedded plot shows the ADC raw data after the digitizer with two bunch trains filled in the ring. The first train had ~3.9 mA filled in 150 consecutive buckets, while the second train had 3.1 mA evenly distributed in 10 bunches, with ~20 ns bunch separations. Two gates were applied to process the beam positions of the two bunch trains as demonstrated in the shaded area.