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Methodology to separate channel conductions of two level vertically stacked SOI nanowire MOSFETs

Bruna Cardoso Paz[a,*], Mikaël Cassé[b], Sylvain Barraud[b], Gilles Reimbold[b], Maud Vinet[b], Olivier Faynot[b], Marcelo Antonio Pavanello[a]

[a] Department of Electrical Engineering, Centro Universitário FEI, São Bernardo do Campo, Brazil
[b] Département des Composants Silicium – SCME/LCTE, CEA-LETI Minatec, Grenoble, France

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ABSTRACT

This work proposes a new method for dissociating both channel conductions of two levels vertically stacked inversion mode nanowires (NWs) composed by a Gate-All-Around (GAA) level on top of an Ω-gate level. The proposed methodology is based on experimental measurements of the total drain current (I_{DS}) varying the back gate bias (V_B), aiming the extraction of carriers' mobility of each level separately. The methodology consists of three main steps and accounts for V_B influence on mobility. The behavior of non-stacked Ω-gate NWs are also discussed varying V_B through experimental measurements and tridimensional numerical simulations in order to sustain proposed expressions of mobility dependence on V_B for the bottom level of the stacked structure. Lower mobility was obtained for GAA in comparison to Ω-gate. The procedure was validated for a wide range of V_B and up to 150 °C. Similar temperature dependence of mobility was observed for both Ω-gate and GAA levels.

1. Introduction

Multiple gate MOSFETs have attracted the interest of semiconductor industry due to strong immunity against short channel effects and great scalability because of improved electrostatic coupling [1–3]. Ω-gate and GAA MOSFETs with nanoscale cross-section, also denominated as nanowires, turned into candidates for future technological nodes due to their performance [2,4]. Such devices are fabricated with close dimensions for both silicon thickness (H_{FIN}) and fin width (W_{FIN}), around 10 nm. In order to fulfill higher drive current requests and increase the on-state current by footprint (I_{ON}/W_{FIN}), nanowires have been recently vertically stacked thanks to advances on tridimensional integration process [5–7]. Once vertically stacked NWs present overall channel width (W_{eff}) proportional to the number of stacked levels (or beams), these devices have higher aspect ratio, which is necessary for NWs to reach industrial targets for saturation current [8].

The implementation of vertically stacked NWs brings technological challenges such as the reduction of intrinsic parasitic capacitance and integration of carriers' mobility boosters. These problems have been recently addressed by the innovative structure fabricated at CEA-LETI, combining inner spacers and SiGe source/drain in vertically stacked p-type NW MOSFETs [7]. The overall effective mobility of these stacked NWs was investigated in [9], while [10] presented a methodology to perform individual electrical characterization of each NW level including explicit expressions for the low field mobility (μ_0) and mobility degradation coefficients (θ_1 and θ_2) dependence on V_B. Once the first work aiming to separate the channel conductions of staked multiple gate devices using V_B [11] does not take into account transport parameters dependence on the back bias, the methodology proposed in [10] improves [11]. In this work, we extend [10] by including experimental measurements and tridimensional numerical simulations of non-stacked Ω-gate NWs varying V_B in order to explain physical effects in the potential, electric field and holes mobility under different back bias conditions. Such explanations are important to understand the vertically stacked NWs behavior and, therefore, sustain the expressions used for mobility dependence on V_B in the proposed methodology, once the bottom level of the stacked structure is Ω-shaped. Moreover, this work brings deeper details of the proposed methodology step by step, so it can be easily reproduced. Discussions concerning temperature influence on V_B dependence are also presented in this work.

The paper is organized as follows: Section 2 details the devices characteristics for both stacked (Section 2.1) and non-stacked NWs (Section 2.2). Section 3 presents the main physical effects of applying V_B on mobility of non-stacked Ω-gate NWs (Section 3.1), the proposed methodology to dissociate channel conductions of two levels vertically stacked NWs (Section 3.2) and temperature influence on V_B dependence

* Corresponding author.
E-mail address: bcpaz@fei.edu.br (B.C. Paz).

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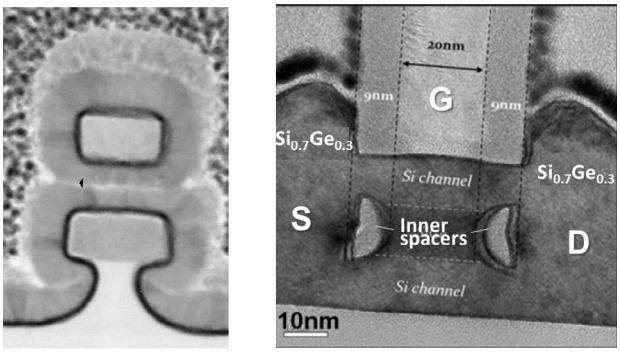

Fig. 1. Vertically stacked SOI nanowire cross section (a) and longitudinal section (b) TEM images.

(Section 3.3). Finally, Section 4 points out the main conclusions of this work.

2. Devices characteristics

2.1. Vertically stacked NWs

Transistors are [1 1 0]-oriented vertically stacked p-type inversion mode nanowires MOSFETs with two levels, being the bottom level Ω-gated and the top level GAA. Fig. 1 shows Transmission Electron Microscopy (TEM) images of the studied stacked NWs cross section (a) and the longitudinal section (b). Usually the vertically stacked NWs have an Ω-gated bottom level while the upper levels are GAA because the fabrication process starts from Fully Depleted (FD) SOI wafers. The first Si channel lies on top of the buried oxide and the upper channels are fabricated on top of SiGe layers, which are replaced after selective etching, giving place to the surrounded gate stack of GAA NWs. From Fig. 1a, it is possible to note that the front gate of the bottom NW is electrostatically coupled with the back gate. Although narrow triple gate MOSFETs present lower back gate bias (V_B) influence in comparison to planar MOSFETs [12], the potential lines coming from the back gate manage to reach the Si channel through the interface between Si and buried oxide. On the other hand, the top NW is independent of V_B because it is surrounded by the gate stack. Despite the lower impact of V_B over the electrical parameters of narrow Ω-NWs, since the bottom NW is V_B dependent while the top one is V_B independent, back biasing can be used as a tool to separate the channels conduction. The interest of using back bias in this work is attached to the methodology proposed in Section 3 to perform individual electrical characterization for future technology optimization.

Devices have been fabricated at CEA-LETI, starting from Silicon-On-Insulator (SOI) wafers with 145 nm buried oxide thickness (t_{BOX}) and using a replacement metal gate (RMG) process to obtain a gate stack composed by HfO_2/TiN/W, resulting in effective oxide thickness (EOT) of 1.15 nm. Each level has a 10 nm thick undoped Si channel and both levels are attached by common metal gate and $Si_{0.7}Ge_{0.3}$:B raised source/drain (B doping level in the order of few 10^{20} cm^{-3} [13]). The transistors have been fabricated in multi finger structures with 50 fins in parallel and channel length (L) of 100 nm. Further fabrication details of the stacked-NWs studied in this work can be found in [7].

Fig. 2 presents drain current, I_{DS} (a), transconductance, g_m (b), and its derivative, $\delta g_m/\delta V_{GS}$ (c), as a function of the front gate voltage (V_{GS}) for stacked NW with W_{FIN} = 15 nm and L = 100 nm, at low drain voltage (V_{DS} = −40 mV), varying V_B from −90 V to 90 V. In these figures the curves with symbols refer to V_B = 0 V. During the measurements, V_B was applied at the substrate of the whole wafer, which is isolated from the active channels by the thick buried oxide. Although ± 90 V may seem like extremely high bias condition, it is important to remember that t_{BOX} = 145 nm. For simplicity, considering the same linear potential drop across the front and back interfaces, 90 V applied at 145 nm-thick oxide would correspond to ~0.7 V applied at the same oxide with thickness of 1.15 nm. The applied back bias values must be adjusted according to the technology of the studied SOI MOSFET to avoid reliability and degradation issues due to high vertical electric field.

Fig. 2a shows expected shift of curves to the left as V_B increases due to threshold voltage (V_{TH}) variation. Moreover, small back conduction is noted in the subthreshold region of logarithmic curves for negative back gate values.

Fig. 2b shows two distinguished peaks for g_m depending on V_B. Results suggests some V_{TH} mismatch between bottom and top levels once the two peaks are still slightly perceived at V_B = 0 V, the first for $V_{GS} \cong -0.4$ V and the second for $V_{GS} \cong -0.75$ V. Two effects are observed and overlapped. First, the g_m peak decreases with V_B increase for negative values (dashed lines) and for high positive V_B (higher than 50 V). Second, for sufficiently low V_B a second g_m peak appears at higher V_{GS} voltages. This second g_m peak presents the opposite behavior from 0 V < V_B < 50 V. The effect that explains the first behavior is related to the effective mobility changing with V_B, which will be detailed in Section 3.1. The second effect happens due to V_{TH} mismatch, the closer both threshold voltages get, the higher the transconductance, once both conductions are overlapped from their starting point, where no strong mobility degradation is observed yet due to surface roughness.

Fig. 2c confirms the existence of V_{TH} mismatch between top and bottom levels at V_B = 0 V. The constant peak in Fig. 2c is insensitive to V_B and related to the threshold voltage of the top NW (V_{TH_GAA}), while the other one is sensitive to V_B and corresponds to the threshold voltage of the bottom Ω-NW ($V_{TH\_\Omega G}$). No peak is observed due to back conduction because of its small contribution, as indicated in Fig. 2a and expected in narrow Ω-NWs. V_{TH} mismatches could be related to charge traps in the GAA-NW, which presents much lower V_{TH} and is more susceptible to defects after RMG process fabrication in comparison to the bottom level.

Fig. 3 shows threshold voltage, V_{TH} (a), and subthreshold slope, S (b), as a function of V_B for stacked NWs with W_{FIN} = 15 and 25 nm and L = 100 nm, at V_{DS} = −40 mV. The threshold voltage has been extracted by the double derivative method. The subthreshold slope has been extracted from $\partial V_{GS}/\partial(\log I_{DS})$ curves, considering an average around the minimum value to account for ~1–2 decades of I_{DS}. Fig. 3a presents V_{TH} for both bottom ($V_{TH\_\Omega G}$) and top (V_{TH_GAA}) NWs extracted from $\partial g_m/\partial V_{GS}$ peaks in Fig. 2c. Threshold voltage mismatches between bottom and top NWs are found to be 0.32 and 0.34 V for W_{FIN} = 15 and 25 nm, respectively, at V_B = 0 V. It is observed that $V_{TH\_\Omega G}$ exhibits a plateau for V_B < −10 V because the back interface of the bottom NW operates in inversion, which degrades the overall subthreshold slope. For V_B > −10 V, the bottom NW enters in full depletion and $V_{TH\_\Omega G}$ decreases linearly with V_B increase, while V_{TH_GAA} remains constant once the top NW is V_B independent. Due to thin silicon layer, the bottom NW never reaches accumulation [14]. At V_B = 50 V, $V_{TH\_\Omega G} = V_{TH\_GAA}$. The NW level with lower $|V_{TH}|$ conducts at lower $|V_{GS}|$ and, therefore, dominates the subthreshold slope behavior of the overall structure. The I_{DS} of the NW level with higher $|V_{TH}|$ is orders of magnitude lower comparing to the other NW level, at a given V_{GS} in the subthreshold regime, so its subthreshold characteristic is hidden in the I-V curve of the overall structure. For V_B > 50 V, $|V_{TH\_\Omega G}| > |V_{TH\_GAA}|$, thus the subthreshold characteristics observed in I_{DS} are determined by the GAA-NW. This explanation is consistent with constant S results varying V_B above 50 V, because GAA characteristics are independent of V_B.

2.2. Non-stacked Ω-NWs

Once the overall behavior of the stacked structure varying V_B is