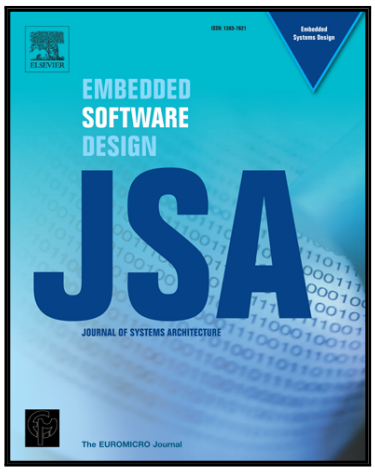

Scheduling Computation and Communication on a Software-Defined Photonic Network-on-Chip Architecture for High-Performance Real-Time Systems

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Scheduling Computation and Communication on a Software-Defined Photonic Network-on-Chip Architecture for High-Performance Real-Time Systems

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This paper presents a novel scheduling approach that efficiently schedules the computational and the communicational resources of a Software-Defined Photonic Network-on-Chip (SD-PNoC) Architecture designed for high-performance real-time systems. The proposed scheduling approach extends the conventional cyclic executive scheduling algorithm from the one that schedules solely the computational resources into a general one that schedules both the computational and the communicational resources together in a synchronized manner. The proposed SD-PNoC architecture employs Software Defined Network (SDN) approach by using application specific conflict-free and contention-free communication patterns to solve the routing and wavelength assignment (RWA) problem exists in photonic networks. The implementations of the collective communication primitives such as broadcast and all-to-broadcast are also presented to demonstrate the system as a whole.

KEYWORDS

Parallel Computer Architecture, Photonic Networks, Routing, Software Defined Network, Optical Circuit Switching, Real-time systems, cyclic executive scheduling

1 INTRODUCTION

In 1965, Moore predicted that the number of transistors fitted onto an integrated chip would double almost every year; 10 years later, he updated his prediction to doubling the number of transistors every two years [1]. If we look back today at the past 10–12 years, we can observe a similar trend in the number of cores in multi/many-core processor architectures. For example, since the first appearance of the dual-core Intel Xeon Processor in 2005, the number of cores in the Intel Xeon Processor has increased to 72 by 2016, almost doubling the number of cores every two years. The physical gate lengths of 7nm that are set in The International Roadmap of Semiconductors (ITRS) has already been achieved [2,3]. Based on the ITRS targets, hundreds or thousands of cores will be fitted into a standard general purpose chip in the near future [4]. Achieving high performance with ever increasing core counts depends on network-on-chip (NoC) architectures that provide high-speed, low-latency communication among those processor cores [5]. These architectures need to be proportionally scalable with the increasing number of processor cores. Even though improvements in the dimensions of silicon semiconducting materials allow the number of processing cores on the chip to increase, the physical boundaries of the metal communication components that interconnect these processors remain insufficient for next-generation processors [6]. The metal communication components will not be sufficient to satisfy the requirements related to high bandwidth and low power consumption. In search of superior solutions, photonic systems on-chip architectures are promising alternative to traditional electrical communication systems. In photonic systems, communication is based on the approach that data is encoded on light waves and transmitted through low-loss waveguides.

Multicore processors have been around for more than a decade; but their utilization in the real-time domain is not overly common. However, emerging high-performance applications in the real-time arena are applying pressure on developers to use multi/many-core processors. Real-time systems are specialized systems wherein performance and accuracy are heavily dependent on timeliness. In real-time systems, system integrity and consistency are related to the timely completion of real-time tasks because a real-time task has to be completed before a predefined time, called the deadline.