Microelectronic Engineering 200 (2018) 45–50

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Research paper

Radiation-tolerance analysis of I-gate n-MOSFET according to isolation oxide module in the CMOS bulk process

Minwoong Lee[b], Seongik Cho[a,*], Namho Lee[c], Jongyeol Kim[b]

[a] Department of Electronic Engineering, Chonbuk National University, 567 Baekje-daero, Deokjin-gu, Jeonju-si, Jeollabuk-do 54896, Republic of Korea
[b] Department of Nuclear Robot and Diagnosis, KAERI (Korea Atomic Energy Research Institute), Daedeok-daero 989-111, Yuseong-gu, Daejeon 34057, Republic of Korea
[c] Department of Radiation Equipment Research, KAERI Advance Radiation Technology Institute, 29 Geumgu-gil, Jeongeup, Jeollabuk-do 52212, Republic of Korea

ARTICLE INFO

Keywords:
Isolation oxide module
Leakage currents
Local oxidation of silicon
Radiation-tolerant n-MOSFET
Shallow trench isolation
Total ionizing dose

ABSTRACT

The n-type metal-oxide-semiconductor field-effect transistor (n-MOSFET) produced in the widely used CMOS bulk process takes radiation damage by the total ionizing dose (TID) effects in radiation environments, so the radiation-tolerant properties of semiconductor integrated-circuits (ICs) used in high-radiation environments is a critical issue. The formation method of the isolation oxide module (IOM), which induces the radiation-induced leakage currents, differs depending on the chip density of the CMOS bulk process. In this paper, we designed and fabricated I-gate n-MOSFETs for bulk process and analyzed the radiation-tolerant characteristics according to IOM. The I-gate n-MOSFET chips are fabricated using the shallow trench isolation (STI) 0.18um and local oxidation of silicon (LOCOS) 0.35um processes of the CMOS bulk process. Tests and evaluation of the TID effects on the chips are carried out by irradiating a total cumulative dose up to 2 Mrad(Si). As the results, in the standard n-MOSFET, the leakage currents of the LOCOS and STI processes are 27.7uA and 16.4uA, and in I-gate n-MOSEFT, are 1.1uA and 0.7uA. The leakage currents of standard n-MOSFET increased by about 25 times before and after irradiation, but the electric characteristics of I-gate n-MOSFET is maintained regardless of the process. Therefore, the process versatility of the I-gate n-MOSFET with the radiation-tolerant performance has been verified.

1. Introduction

Today, a radiation damage of electronic systems used in high radiation environments such as space, nuclear power, and military part, not only results in significant cost and power losses, but also has a direct impact on human life. Particularly, when radiation damage occurs in Integrated circuits (ICs) used in a safety/control measuring system of the nuclear power plant or a communication/video image taking/track setting system of the satellite, the ICs has an upset causing a data error, or a latch-up by the operation of a parasitic thyristor in the electronic device. The latch-up can be extended to a burn-out, an irreversible permanent damage of the device, which can lead to functional paralysis throughout the electronic system [1,2]. Accordingly, the radiation-hardening technology of electronic devices is becoming more important.

The radiation-induced damage process of a silicon-based CMOS IC causes various phenomena depending on the radiation type, the total dose, the flux, and even the load type in the device. These are a neutron effect, a total ionizing dose effect (TID), a transient dose effect (TDE) and a single event effect (SEE) [2,3].

Among these phenomena, particularly, a TID effect degrades the characteristic of the n-type MOSFET constituting the CMOS IC by gamma rays accumulated over a long period of time. When silicon-based electronics exposed to the TID effect, the MOS structure experiences ionization by cumulative radiation and electron-hole pairs (EHP) are formed on the silicon oxide film [4]. Generally, since a positive bias is applied to the gate of CMOS, the electrons move toward the gate electrode and the holes move toward the silicon body. At this time, the electrons easily disappear due to the tunneling effect since they have high mobility, but heavy holes accumulate at the interface of the silicon oxide film. The accumulation of the holes occurs on the thick isolation oxide film between the n-MOSFET source and drain in the CMOS structure. The accumulated holes called fixed charges induce electron channels, which in form leakage current paths between the drain and source in cut-off region of the n-MOSFET as shown in Fig. 1. The TID effect attenuates the properties of the n-MOSFET, resulting in overall malfunction, and is responsible for problems with electronic devices and system composed of CMOS [4,5].

* Corresponding author.
E-mail address: sicho@jbnu.ac.kr (S. Cho).

https://doi.org/10.1016/j.mee.2018.08.007
Received 15 March 2018; Received in revised form 7 August 2018; Accepted 28 August 2018
Available online 11 September 2018

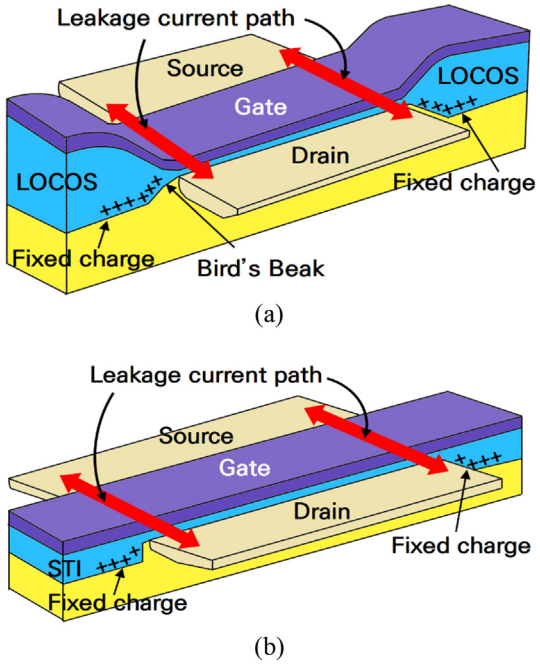

Fig. 1. Leakage current path between source and drain in standard n-MOSFET structure with (a)LOCOS and (b) STI process.

When electronic devices in the electronic systems used for the nuclear power plants or satellites are exposed to the TID effects, it can result in significant damage due to malfunctions. However, detecting such the malfunctions can be difficult, and there are considerable limitations to replacing or fixing internal electronic devices [6,7]. In order to reduce such damage from the TID effects, research has been carried out to identifying commercial devices with high tolerance to cumulative radiation, and enhancing radiation tolerance through shielding.

However, this research is not a fundamental solution because it is an indirect method, not the radiation-hardening of the device itself. In addition, it is inefficient and limited because it requires a lot of cost and time by the repetitive irradiation test and shielding materials of each device. For this reason, in order to systematically solve the radiation damage of electronic devices, it is necessary to study radiation-hardening from the minimum unit device level. A layout modification technique corresponding to the radiation-hardening technology in the device level has been actively studied recently because it can be achieved only by commercial CMOS process. The layout modification technique can design the radiation-tolerant unit device(CMOS) by using the commercial process procedure as it is, and it is possible to reduce the period and the expense when expanding to the electronic circuit or system based on the radiation-tolerant unit device [8].

The isolation oxide module (IOM), which induces the TID effects, is a module that physically and electrically isolates devices on the wafer. When isolation between devices is not properly isolated, punch-through or break down can occur, resulting in the malfunctioning of devices within the IC chip. As the channel length has been steadily reduced through process improvements, the LOCOS [9] and STI processes have been used as the IOM formation methods [10,11]. The fabrication process differs depending on the application because the IC supply voltage and properties vary. Consequently, the IOM differs and results in differences in the leakage current path, the leakage current, and the n-MOSFET properties, depending on the total cumulative dose.

Radiation-tolerant unit devices fabricated with the latest commercial processes include the enclosed layout transistor (ELT) [12] and dummy gate-assisted (DGA) n-MOSFET [13]. The DGA and ELT structures have only changed their layout, so they have the advantage of not needing additional circuit or process steps and having radiation tolerance. But they have the disadvantage of requiring the remodeling of the width/length (W/L) ratio, and limitations in circuit design [14]. The I-gate n-MOSFET is an improved structure with utilizes a layout modification technique. The I-gate n-MOSFET exhibits high radiation tolerance, does not require remodeling of the W/L ratio, and is flexible in that the circuit design is simple [15].

In this study, an I-gate n-MOSFET is designed using the commercial CMOS 0.18um STI process and 0.35um LOCOS process. Its radiation tolerance was analyzed according to the IOM for each process using evaluation testing for the TID effects. The goal of the study is to develop enhanced radiation tolerance for electronic devices utilized in satellites and nuclear power plants.

This paper is structured in the following manner. Section II explains the radiation-tolerant I-gate n-MOSFET structure and the design of the I-gate n-MOSFET for each process. Section III compares and analyzes the radiation-tolerance properties of the I-gate n-MOSFET for the STI and LOCOS processes using TID effects testing, and finally, Section IV details the conclusions obtained in this study.

2. Radiation-tolerant n-MOSFET design

2.1. I-gate n-MOSFET structure

Among the radiation-tolerant electronic device technologies, the layout modification technique is advantageous with respect to both time and cost savings, because the technique utilizes existing commercial processes without additional steps [8]. The I-gate n-MOSFET fabricated with this technique was designed based on the n-MOSFET layout of a conventional commercial process. As shown in the Fig. 2, the I-gate n-MOSFET layout structure changed the gate poly layer to an 'I' shape, secured space between the isolation oxide and the source or drain, and added the p + and p-act layers, which increased the threshold voltage (V_{TH}).

These changes prevent channel inversion, which occurs due to the accumulation of electron holes on the silicon oxide film, by blocking leakage current paths. Also, the p-act layer was set to meet the N-active layer to prevent the formation of a thick isolation oxide film which accumulates electron holes, thereby blocking the leakage current paths between the source and drain.

Each layer was added/changed to enhance the radiation tolerance of the device. By making the semiconductor devices radiation-tolerant, it is possible to make the entire IC composed of semiconductor devices radiation-tolerant. Unlike previous layout modification techniques applied to the n-MOSFET, the proposed I-gate n-MOSFET has the advantage of not requiring additional size remodeling, since the I-gate n-

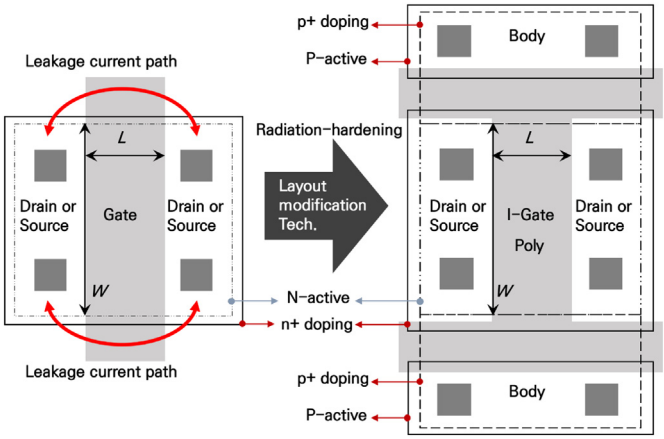

Fig. 2. Radiation-tolerant I-gate n-MOSFET structure with the layout modification technique [15].