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Calculation of the number of modules and the switching frequency of a modular multilevel converter using near level control

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ABSTRACT

This paper is focused on the modular multilevel converter (MMC) topology that uses the near level control (NLC) method. Specifically, it addresses the relationship between the number of levels or switching modules, the switching frequency and the harmonics superimposed on the generated voltages and currents, making a comparison with the high and medium voltage AC codes. Furthermore, it also assesses the possibility of connecting the MMC to the electrical grid without using any coupling inductor, either using a transformer or simply directly. Finally, it shows how to automate the simulations necessary to select the number of levels and the switching frequency.

1. Introduction

MMC topology has drawn the attention of the R&D community and of the industry in the last few years. Its main application is high voltage DC transmission (HVDC), but there are also others related to its ability to control the DC current in the case of a DC bus short-circuit, etc.

Many papers have recently been published addressing such subjects as capacitor balancing [1,2], voltage modulators [3], converter modeling [4], circulating current reduction [5], direct current (DC) fault handling capability [6], control under unbalanced voltage conditions [7], among others.

The most important electrical grid installers have chosen the MMC topology as the most suitable for HVDC transmission [8] and one of the most important recent applications has been offshore wind parks [9].

MMCs can be controlled in high frequency using several types of modulation, or in low frequency, by using the near level control (NLC) algorithm [10]. The latter is preferred in high power applications because of its lower power losses in the semiconductors.

MMCs (Fig. 1) are made up of three phases, where each phase is split into an upper and a lower part made up of an arm and one inductance. The arm comprises n switching modules (SM). In turn, each SM comprises, in the half bridge (HB) topology, two IGBTs, two diodes and one capacitor.

The choice of the number n of SM has important consequences in the NLC algorithm. When n is high, alternating current (AC) voltages are made up of many steps and their total harmonic distortion (THD) is low. Because all the SM are identical, increasing the number of levels does not increase the power electronics by very much, but it does increase the complexity of the control due to the high number of control signals to be handled. Systems to reduce the complexity of the communications are currently still under study [11].

Each country has its own grid code related to the current and voltage harmonics that the MMC must fulfill. These codes are more restrictive as the voltage and current increase, and they establish the limits for the THD and for the individual harmonics. There are several aspects that influence the harmonic level: the number of SM, switching frequency, and the in-series inductance (sum of the coupling inductance used by the MMC, the transformer leakage inductance and the electrical line inductance).

This paper aims to provide answers to several questions related to MMCs that use NLC: How many SM should be used? What switching frequency? Is it necessary to use a coupling inductor, or is it sufficient to use the transformer leakage inductance, or it can even be directly connected to the grid?

The following features are desirable when designing an MMC:

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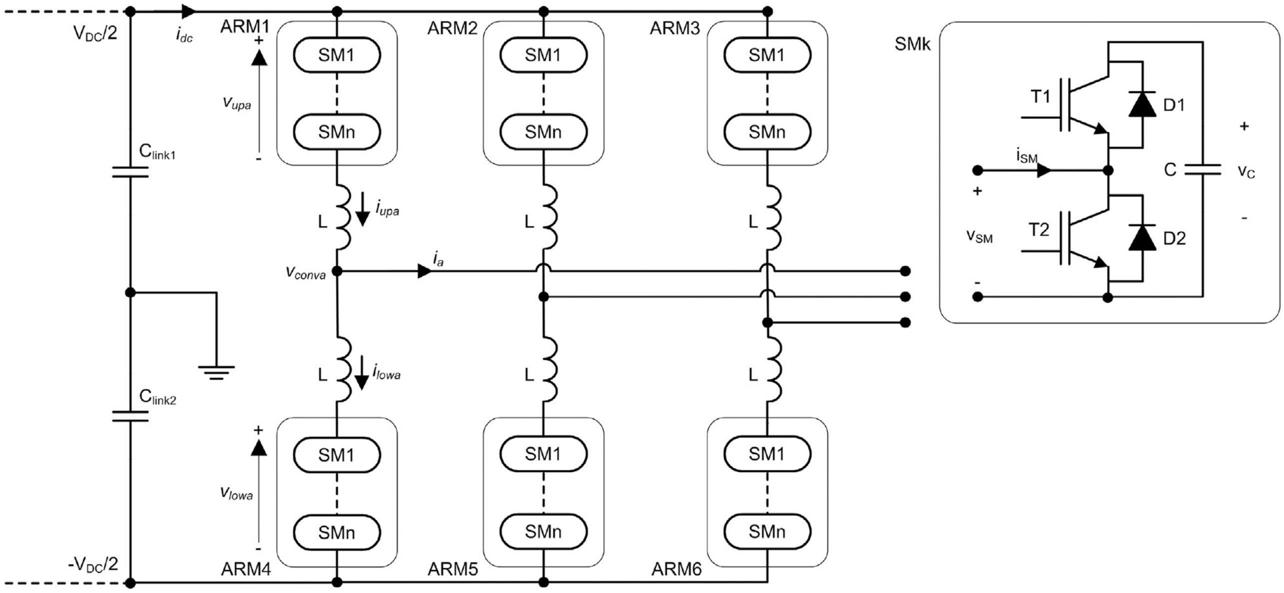

Fig. 1. Modular multilevel converter (MMC) scheme and half-bridge switching module (HB-SM) structure.

- Using a low number of SM can reduce the complexity of the control hardware (buses with a lot of cables) and also the software complexity (communication system between the central control and each module control). However, this probably helps to generate high voltage and current harmonics that can exceed the grid code limits.
- Reducing the number of SM, in order to make the control simpler and reduce the cost, allows the use of this electronic converter in low power applications. Indeed, a low number of SM and an effort to integrate power electronics + control hardware + communications makes it easier to use in low cost and low rated power applications. They can even be packaged in one or several big chips, as is done with the low power IGBT bridges.
- Using a low switching frequency to reduce the switching losses and the complexity of the control. The limit is then the harmonics in voltages and currents.
- Removing the coupling inductor (and even the coupling transformer). This depends on the level of harmonics present in the output voltage, and the transformer and line inductances.
- For a given number of levels, determine the maximum switching period limited to getting just one level step in the output voltage.

This study is carried out using analytic techniques and simulations in Matlab/Simulink. The waveforms are generated depending on the number of SM and the switching period, after which the harmonics are calculated. Depending on the line inductance value, the current harmonics are then studied. Finally, a methodology is developed that automates the Matlab/Simulink simulations and the results obtained.

The paper is organized as follows. Firstly, Section 2 presents the fundamentals of MMC and NLC. In Section 3, the maximum allowed value of the commutation period is calculated. In Section 4, the voltage and current harmonics are calculated as a function of the number of SM and the commutation period. Sections 5 and 6 show detailed MMC numeric and real time simulations aimed at validating the previous harmonics calculations. Finally, the conclusions of the paper are presented.

2. Fundamentals of modular multilevel converters and near level control

2.1. Fundamentals of MMC

The simplest SM topology (Fig. 1) is called half-bridge (HB). It comprises two IGBTs, two diodes in anti-parallel configuration and one capacitor. There are other more complex topologies that perform better in cases of short-circuits, such as full bridge (FB) and the double clamp submodule topology [12].

The SM operation can be explained using the HB topology (Table 1). When the SM is in the ON state, T1 is also ON and T2 is OFF; depending on whether the current i_{SM} is positive or negative, the capacitor voltage v_C rises or falls respectively. When the SM state is OFF, T1 is also OFF and T2 is ON; then, the capacitor voltage remains constant, independently of the sign of the current i_{SM}.

Table 1
Relationship between the elements and variables of the SM.

SM state	T_1 state	T_2 state	i_{SM}	Δv_C	i_{SM} flows through	v_{SM}
ON	ON	OFF	> 0	+	D_1	v_C
ON	ON	OFF	< 0	−	T_1	v_C
OFF	OFF	ON	> 0	0	T_2	0
OFF	OFF	ON	< 0	0	D_2	0

The sum of the number of SMs in the ON state in the upper arm n_{up} and in the lower one n_{low} is equal to the number n of SMs per arm,

$$n_{up} + n_{low} = n \tag{1}$$

The equations that establish the relation between the DC voltage V_{DC}, the output voltage v_{conva}, the voltages in the upper arms v_{upa} and in the lower ones v_{lowa}, as well as the currents in the upper arms i_{upa} and in the lower ones i_{lowa} (Fig. 1), are:

$$v_{conva} = \frac{V_{DC}}{2} - v_{upa} - L\frac{di_{upa}}{dt} \tag{2}$$

$$v_{conva} = -\frac{V_{DC}}{2} + v_{lowa} + L\frac{di_{lowa}}{dt} \tag{3}$$

where the voltages in the upper and lower arms depend on the ON/OFF state of each upper SM $S_{upak} = 1/0$, or lower SM, $S_{lowak} = 1/0$, and on the voltage in every SM of the upper arms v_{Cupak} and lower arms v_{Clowak}.

$$v_{upa} = \sum_{k=1}^{n} S_{upak} v_{Cupak} \tag{4}$$