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# Removing overhang and increasing atom re-deposition of sputtering to enable gap-filling scalability

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ABSTRACT

Semiconductor manufacturing has reached sub-10-nm technology nodes, and nanoscale gap filling has become an emergency critical requirement for memory with high density and low power consumption. However, it is limited by the non-conformal deposition of current sputtering techniques, such as physical vapor deposition, despite its high quality, low impurity level, and good composition controlling. Here, we present an excellent void-free gap filling results for sub-10-nm nano-pores, and extend the gap-filling limitation of the conventional sputtering technique by the deposit-etch-deposit (DED) method. Coupled with investigating the DED mechanism via the experimental measurements on the nano-pores with different sizes, results indicate that the overhang is removed and atoms are re-deposited during the etching step, which are critical factors for DED process. DED parameters including deposition, etching, and cycling times are investigated and optimized comprehensively. Furthermore, element uniformity and electrical performance are comparable between DED and conventional sputtering technique and have little difference. These results demonstrate that the DED technique, owing to its flexibility and low-cost application compared to conventional sputtering tools, is a potential nanoscale gap-filling solution for sub-10-nm technology nodes.

## 1. Introduction

Phase-change memory (PCM) has tremendous advantages over conventional solid-state memory due to its non-volatility, high speed, and scalability. Nevertheless, for shrinking a device size to nanoscale, higher density and lower power consumption is required in order to extend PCM into dynamic random access and storage class memory [1–3]. There are mainly two fabrication schemes of nanoscale PCM cells: 1) define the thin-film pattern of $Ge_2Sb_2Te_5$ (GST) on a blanket wafer using a dry-etch process, and 2) fill a nano-pore with GST followed by a chemical-mechanical polishing (CMP) process to remove the GST outside the nano-pore. In the gap-filling case, GST is usually filled in a nano-pore by atomic layer deposition (ALD) [4–6], metal-organic chemical vapor deposition (MOCVD) [7–9], and physical vapor deposition (PVD) [10,11]. However, for dry-etch process of GST, it is difficult to etch a pattern with sub-10-nm size due to the etching damage of GST sidewall [10–12]. For the ALD and MOCVD processes, gap filling of GST with void-free performance has been achieved on nano-pores with a bottom critical diameter (CD) of 7 nm, but the disadvantages of high impurity level and poor composition controlling restrict its application in PCM despite its good gap-filling capability [13–15]. Currently, conventional PVD is the mainstream method for phase-change material deposition due to its high purity and accurate composition controlling, but its step coverage capability is worse than ALD and MOCVD. In the semiconductor process flow, PVD is generally applied to obtain uniform step coverage (such as barrier/seed) instead of full filling [16–18]. Recently, some gap-filling results for GST based on the PVD technique have been presented [19–23]. Kikuchi et al. reported a GST depositing method by long throw sputtering tool with optimized substrate bias and found that it can be used to fill the hole with a bottom CD of several hundred nanometer [19]. An in-situ deposition-etch sputtering method and a full filling result on a nano-pore with a bottom CD of 50 nm were presented by Cho et al. [20], and electrical performance of the confined cell was also qualified. However, mechanism of the filling process was not introduced. As for the deposit-etch-deposit (DED), Ren et al. have studied the process and tried to

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discuss the mechanism of DED process with a bottom CD of 30 nm. They predicted that DED process could be a potential gap-filling solution for 45 nm and below technology nodes [21,23]. However, the systematic study of DED and its mechanism still need to be investigated, specifically for sub-10-nm technology nodes based on the PVD technique.

In this paper, we investigate the conventional PVD technique and its limitations, and then introduce DED technique for nanoscale gap filling and discuss its related mechanism. The DED technique's process parameters, related to deposition, etching, and cycling times, are comprehensively investigated. Eventually, the void-free gap filling and element uniformity are characterized, which may be a potential nanoscale gap-filling solution for sub-10-nm technology nodes.

## 2. Experimental details

### 2.1. Sample preparation

GST film was deposited using the direct current (DC) pulsed method and etched by inductively coupled plasma (ICP) soft etching in a 300-mm magnetron sputtering system at room temperature. The GST deposited at room temperature keeps amorphous state, its adhesion between GST film and substrate is much better, which is critical for controlling of the following processes. A radio-frequency (RF) generator (13.56 MHz) was used to initiate the plasma with argon gas. The background pressure of the sputtering system was $3.4 \times 10^{-6}$ Pa. To study the step coverage challenge of conventional sputtering process, GST film with the thickness of 430 nm was sputtered onto patterned wafers, which have been etched on $SiO_2$ film to form nano-holes with different bottom diameter (170, 300, 450, 650, and 1050 nm) and fixed depth as 200 nm. The step coverage of GST was checked by cross-sectional images and calculated using the GST film thickness at the bottom of nano-pore divided by the deposition thickness of 430 nm on the top. The parameters of the DED process were tuned to optimize the gap-filling performance for GST, and the parameters of the deposition and etching steps were optimized by tuning the power from 60 to 400 W and the argon gas flow from 15 to 150 sccm. The DED technique was introduced to fill the nano-pore with a bottom CD of 7 nm/30 nm and an aspect ratio (AR) of 1.5. The DED process parameters, relating to deposition (power, pressure, and thickness), etching (power, pressure, and etching amount), and deposit-etch cycling times, were investigated and optimized. Here the etching amount was defined as the etch percentage to the deposition thickness. During the DED process, the etching steps are carried subsequently after the GST deposition without vacuum break during the switch between sputtering and etching chambers, which can effectively prevent GST from being oxidized by the Oxygen in the air. The samples of DED process qualification were prepared on the $Si/SiO_2$ (400 nm) with GST depositing 50 nm/etching 10 nm/depositing 50 nm/etching 10 nm/depositing 20 nm, which was compared with single deposition at 100 nm to check the composition shift and electrical performance.

### 2.2. DED technique characteristics

The gap-filling performance was characterized by the cross-sectional images of scanning electron microscopy (SEM) and transmission electron microscopy (TEM). Line scanning using energy-dispersive X-ray spectroscopy (EDX) of TEM was applied to check the elements' uniformity in the fully filled nano-pore. The composition variation and electrical performance on blanket wafers were compared between single-deposition and two-cycle DED by glow-discharge optical emission spectroscopy (GD-OES) and resistance-temperature (*R-T*) curves by the four point probe (FPP) technique accordingly.

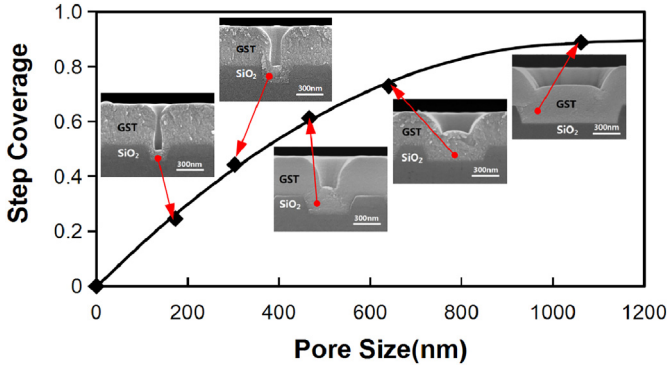


**Fig. 1.** Step coverage challenge of the conventional sputtering process with the bottom diameter of hole shrinking from 1050 to 170 nm and the depth of hole is fixed as 200 nm.

## 3. Results and discussion

### 3.1. Challenge of PVD step coverage with scaling down of the device

The conventional PVD technique cannot fully fill the nano-pore for the PCM [24–26]. GST film with the thickness of 430 nm was sputtered onto patterned wafers, and the nano-holes with different bottom diameter (170, 300, 450, 650, and 1050 nm) and fixed depth as 200 nm were filled by the conventional PVD technique. The step coverage of GST was checked by cross-sectional images inserted in Fig. 1 and calculated using the GST film thickness at the bottom of nano-pore divided by the deposition thickness of 430 nm on the top. Obvious decreasing of step coverage was found from 0.89 to 0.25 with decreasing pore size from 1050 to 170 nm. The holes with bottom diameter bigger than 450 nm were easily fully filled. And the pore with a bottom CD of 300 nm can be marginally fully filled. Furthermore, Overhang at the top corner of the nano-pore became much more severe for smaller holes with CD of 170 nm, which has induced bad step coverage at the bottom. Therefore, the step coverage requirement of sputtering technique is trended to be much more challenging with the shrinkage of the bottom diameter of nano-pore. However, conventional PVD cannot work well for much smaller pores, because the sputtering technique is a non-conformal deposition process and easily creates overhang due to atom scattering at the top corner of the pore during sputtering, which prevents the GST atoms from filling into the pore bottom. This trend will be further enhanced at sub-10-nm technology nodes. An open profile of nano-pore can suppress the overhang growth and facilitate better gap filling, but will degrade the programming efficiency and induce high power consumption [27–30]. Therefore, a new gap-filling technique must be urgently developed for pores with CD values on the sub-10-nm scale.

### 3.2. DED process concept

The DED technique was developed as a gap-filling solution for sub-10-nm technology nodes based on the PVD technique due to its good scalability. As shown in Fig. 2(a), after the first deposition, severe overhang at the top corner was the critical gap-filling issue for the conventional PVD technique, which prevented the bombarded GST atoms from filling into the pore bottom. An additional etching step followed the first deposition step to remove the overhang simultaneously, and the atoms being bombarded out from the overhang area entered the pore and were then re-deposited at the pore bottom or corner. So the pore profile is re-defined: the bottom area was better filled and the top profile became more open as shown in Fig. 2(b), which is benefit for GST atoms being filled into the nano-pore during