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$SrTa_2O_6$ induced low voltage operation of InGaZnO thin-film transistors

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ABSTRACT

High-k amorphous $SrTa_2O_6$ (STA) thin films were successfully deposited by rf magnetron sputtering for gate insulators in thin-film transistor (TFT). Practical STA thin films with high dielectric constant of 41.8, wide band gap of 4.58 eV, and low leakage current of $\sim 10^{-8}$ A/cm^2 were obtained through by optimal sputtering condition. The TFTs with amorphous InGaZnO (IGZO) as a channel and STA as a gate insulator were fabricated and investigated for thinning effects of gate insulator on transfer characteristic. The IGZO-TFT with 70-nm-thick STA achieved high performance switching properties; (mobility of 14.9 cm^2/(V·s), threshold voltage of 0.6 V, sub-threshold swing of 111 mV/decade, and on/off ratio of 1.0×10^{10}). These characteristics are due to the large gate capacitance of 4.6×10^{-7} F/cm^2 and low gate leakage current from use of STA.

1. Introduction

Among various electric devices, thin-film transistors (TFTs) are key future devices, not only for flat panel display, but also for wearable and flexible applications. Recently, TFTs with In_2O_3 and ZnO based oxide semiconductors as a channel layer have been attracting researcher's attention as a candidate for next generation displays with additional functions; for example, higher resolution, lower power consumption, flexibility and transparency. Among these TFTs, amorphous InGaZnO (IGZO) is a promising material because of its many advantages; such as, high mobility over 10 cm^2/(V·s), low leakage current at off region, transparency due to its wide band-gap about 3.0 eV, and low fabricating temperature [1–4]. However, IGZO-TFT requires high operation voltage to achieve high device performance [4]. Generally, gate voltage (V_{gs}) over 10 V must be applied to obtain practical on-current, field effect mobility (μ_{FE}), and on/off ratio. This high operation voltage was limited by SiO_2 or SiN_x gate insulator due to their low dielectric constants, which hinders the power saving of device. To solve this issue, increasing the gate capacitor (C_i) is indispensable to decreasing V_{gs} as operation voltage. Recently, various high-k dielectric oxides have attracted a great deal of attention as a material for gate insulators to achieve low voltage operation [3,5,6]. In previous reports, many researchers have demonstrated that use of traditional high-k dielectrics such as Y_2O_3, ZrO_2, HfO_2, Al_2O_3, TiO_2, La_2O_3, and Ta_2O_5 can improve the operation voltages, μ_{FE} and sub-threshold swings (S.S.) [3,5–19]. In addition, the multi-component dielectrics such as $Ba_{0.5}Sr_{0.5}TiO_3$, MgO-$Ba_{0.6}Sr_{0.4}TiO_3$, $SiTiO_2$, HfLaO, LaTaO, $HoTiO_3$, $GdTiO_3$, NbLaO, and $SrTa_2O_6$ were also studied to improve TFT performance [15,18,20–27]. However, a part of these TFTs have critical weak points such as high gate leakage current and high leakage current at off region due to its poor insulation property, which causing degeneration in device stability, reliability and reproducibility. Furthermore, abnormal device parameters are obtained when the gate leakage current is high [28]. Thus, we consider selection of suitable material and optimizing fabrication conditions is necessary to realize high performance TFT.

In our previous reports, we focused on high-k $SrTa_2O_6$ (STA), which has a high dielectric constant of 30–40 in the amorphous state, low leakage current of $\sim 10^{-8}$ A/cm^2, and wide band-gap of 3.9–4.7 eV [27,29–34]. Thus, we consider STA as a promising material because it satisfies the high dielectric constant with high insulation property applied for gate insulator in TFT. The STA thin films have been mainly fabricated by atomic layer deposition, chemical vaper deposition, atomic vaper deposition, and sol-gel method [29–32,35–43]. Compared with the solution process, these vacuum processes ensure deposition of high quality and purity films [29–31,35]. In contrast, few studies on STA using rf magnetron sputtering have been reported. Thus, we have been deposited STA by sputtering method and shown that the use of STA as a gate insulator is effective for improving the operation voltage in IGZO-TFT [27]. This TFT showed a low gate leakage current, which is mostly comparable to thermally grown SiO_2 gate insulators.

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Additionally, it showed accurate characteristics not affected by leakage current. In this way, we demonstrated that sputtering is a promising method for depositing STA thin film. Generally, the properties of gate insulators (i.e., leakage current, dielectric constant and surface morphology) have a great influence on the TFT characteristics. Therefore, optimizing fabrication conditions is necessary for TFT application. In addition, the higher dielectric properties of STA thin films are necessary to obtain higher performance TFT. However, detailed sputtering conditions of STA have not been sufficiently clarified because there are few reports. In this work, we examine the effects of sputtering conditions (e.g., substrate temperature and working pressure) on the film properties, such as dielectric property and surface morphology were investigated. Additionally, we also report performances of low voltage operating IGZO-TFT with the sputtered STA gate insulator.

2. Experimental methods

The amorphous STA thin films were deposited on Pt/TiO_x/SiO_2/Si (Pt/Si) substrates using a $SrTa_2O_6$ ceramic target by rf magnetron sputtering method. The thickness of STA thin films in this experiment was set about 150 nm for characterization. The sputtering conditions of STA (i.e., target-substrate distance, rf power, working pressure, O_2 partial pressure, and substrate temperature) were 80 mm, 80 W, 0.2 or 2.0 Pa, 50.0%, and 200 to 400 °C, respectively. To measure leakage current density–electric field (J–E) and capacitance–frequency (C–F) properties, Pt/STA/Pt/Si structure was used, which corresponds to the metal–insulator–metal (MIM) capacitor. The top electrodes of Pt were deposited though a metal mask by dc sputtering. Finally, these MIM devices were annealed at 300 °C for 60 min in air.

In this work, a top-contact and bottom-gate type TFT structure as shown Fig. 1 was adopted. As a gate insulator, the 70- and 100-nm-thick STA was deposited by sputtering. After deposition, STA thin films were annealed at 500 °C in O_2 with moisture atmosphere using a tubular furnace. As a channel layer, the 70-nm-thick amorphous IGZO was deposited on STA gate insulators using a $In_2Ga_2ZnO_7$ ceramic target by sputtering. The sputtering conditions of IGZO (i.e., rf power, working pressure, O_2 partial pressure, and substrate temperature) were 100 W, 0.6 Pa, 4.5%, and room temperature, respectively. As the source and drain electrodes, the 20 nm/80 nm-thick Pt/Mo laminated thin films were deposited by rf sputtering. The channel width (W) and length (L) were set as 90 μm and 10 μm, respectively. The TFT structure was patterned by wet-etching, photolithography and lift-off processes. Finally, the fabricated TFTs were annealed at 290 °C in O_2 atmosphere for 30 min and 300 °C in air atmosphere for 120 min.

The surface morphology was observed by the atomic force microscopy (AFM; Shimadzu SPM-9600). The chemical composition ratio was analyzed by X-ray photoelectron spectroscopy (XPS; ULVAC-PHI PHI5000 VersaProbeII). The optical property of STA thin films was evaluated by optical spectrometer (Jasco V570). The J–E and C–F properties of STA films were measured by precision source/measure unit (Agilent B2902A) and LCR meter (NF ZM2376), respectively. The characteristics of the TFTs were measured by a semiconductor device analyzer (Agilent B1500A).

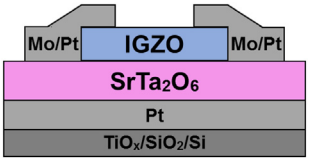

Fig. 1. The cross-sectional image of fabricated top-contact and bottom-gate type TFT with IGZO channel and STA gate insulator.

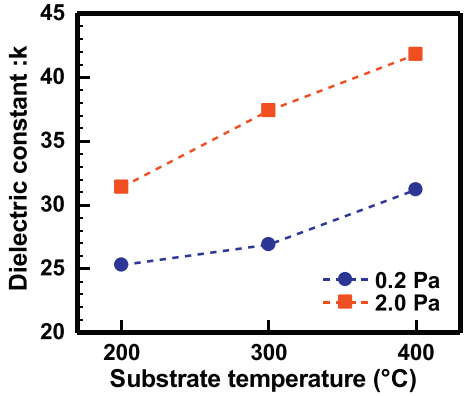

Fig. 2. The dielectric constants of STA thin films deposited at various substrate temperature and working pressure.

3. Results and discussion

3.1. Deposition and characterization of $SrTa_2O_6$ thin films

In the gate insulator, the uniform amorphous state is required to prevent leakage current from grain boundaries. The crystallization temperature of STA is reported as 700–800 °C [27,29,31,32]. Thus, all STA thin film is in amorphous state because the maximum temperature for fabricating TFTs is 500 °C in this work.

Fig. 2 shows the dielectric constants of STA thin films deposited under various sputtering conditions. The dielectric constants were calculated from the C–F property obtained from MIM capacitors. The dielectric constants of amorphous STA thin films deposited at 2.0 Pa are 31.4, 37.4, and 41.8 for substrate temperatures of 200, 300, and 400 °C, respectively. Additionally, the dielectric constants of STA thin films deposited at 0.2 Pa are 25.3, 26.9, and 31.2 for substrate temperatures of 200, 300, and 400 °C, respectively. These values are almost the same as values previously reported [27,29–32]. From Fig. 2, it is apparent that the dielectric properties greatly depend on the sputtering conditions. It was confirmed that the dielectric constants improved with increasing substrate temperature. In addition, the dielectric constants differ by over 10 between 2.0 Pa and 0.2 Pa. Thus, the chemical composition ratio of the STA thin films deposited at 400 °C with different working pressure was analyzed by XPS. The chemical composition ratios are Sr/Ta = 0.54 and Sr/Ta = 0.73 for samples deposited at 2.0 Pa and 0.2 Pa, respectively. Thus, this result suggests that the difference in dielectric constant is caused by compositional deviation. Similar behavior has been confirmed in another report [31].

Generally, the surface morphology of a gate insulator is important factor to achieve high device performance, because it provides good electric properties and prevents deterioration of S.S. and μ_{FE} [5,13,15,16,25,26,44,45]. Thus, the surface morphologies of STA thin films were also investigated using AFM. In this work, the surface morphology was evaluated using root mean square (r.m.s) roughness. Figs. 3 and 4 shows surface morphologies and r.m.s. roughness values of STA thin films. The measured region is 1 μm × 1 μm. From these results, the surface morphologies without cracks and precipitates were observed. Thus, these AFM image and r.m.s. values successfully reflected the surface morphology of STA thin films. The influence of the working pressure on the surface roughness was slight, and the influence by the substrate temperature was great. Smoother surfaces with r.m.s = 0.74 nm (2.0 Pa), 0.81 nm (0.2 Pa) were obtained from substrate temperature of 200 °C. In contrast, the rough surfaces with high r.m.s. values over 1.5 nm were obtained from a substrate temperature of 300 °C. Additionally, the STA deposited at the substrate temperature of 400 °C showed about 1.0 nm. However, these surfaces are rough than the thermally grown SiO_2 used for gate insulator. Thus, we consider that influence of difference in surface morphologies on TFT