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A Low-Cost High-Speed Self-Checking Carry Select Adder with Multiple-Fault Detection

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Abstract

Employing cost-efficient, high-speed and fault-tolerant processing units is an essential goal in the design of current processors. In this paper, the carry select adder (CSeA) as one of the fastest adders is augmented respecting multiple-fault detection, delay, power and required area. In this way, based on the concept of a self-checking full adder, an *m*-bit logic-optimized self-checking single-stage CSeA is designed in which at most *m* concurrent faults can be detected. Then, based on a delay analysis, a new grouping structure for the self-checking multi-stage CSeA apart from the conventional square-root (SQRT) grouping is proposed to optimize the overall delay for different adder sizes. The proposed grouping structure decreases the power overhead, as well. Experimental results show that as well as an acceptable multiple-fault detection capability, noticeable improvements are achieved in delay and power consumption compared to the previous self-checking CSeA designs. The proposed CSeA reaches in average 20% power reduction and 34% speed improvement in different sizes compared to the best existing design.

Keywords: Carry select adder; Self-checking adder; Fault/error detection; Multiple faults, Fault-tolerance

1. Introduction

Nowadays, the VLSI systems are more encountering both transient and permanent faults because of the factors such as shrinking power supply voltages and diminishing transistor feature sizes. In fact, the vulnerability of such systems against different environmental effects is increasing especially in the extreme environments such as the outer space. Therefore, the VLSI-based circuits especially the processors should be reconsidered to be reinforced against different types and numbers of faults in the form of fault masking or fault detection. Regarding the fault detection property, the concept of self-checking is used which includes fault-secure and self-testing characteristics, and such a system is called totally self-checking [1]. A circuit is said fault-secure if it remains unaffected by a fault or it indicates a fault as soon as it occurs [1]. In addition, a circuit is said self-testing if it is guaranteed that for each modeled fault there is at least one input vector, occurring during the normal operation of the circuit that detects it [2].

To attain self-checking processing systems, the concepts of self-checking and error detection have been applied on a variety of adders [3-7] and some multipliers [8-12] although these concepts are used