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Impact of Substrate Bias and Dielectrics on the Performance parameters of Symmetric Lateral Bipolar Transistor on SiGe-OI for Mixed signal applications

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Abstract

In our strive to improve upon low power high speed devices for digital and mixed signal applications, Symmetric Lateral Bipolar Transistor has come out as a promising candidate and gained importance of late. Researchers in the field have shown improved performance parameters with this novel device for digital and analog applications. We investigate for the first time the impact of substrate bias for symmetric lateral bipolar transistor on Silicon Germanium on Insulator (SiGe-OI) with varying thickness of active device area (T_{SiGe}), thickness of BOX layer (T_{Box}) and k-values of dielectric BOX layer for analog/mixed signal applications. We optimize our design in terms of major performance parameters like gain and f_T by varying parameters like T_{SiGe}, T_{Box} and k-values of dielectric BOX under substrate biased condition. We were able to achieve an improvement in gain and f_T (in GHz) by almost 41.7 percent @ $I_C \approx 1\mu A/\mu m$ and 1.4 percent respectively by increasing the k-value of BOX from 3.9 to 22 with substrate bias. We studied for the first time complementary symmetric lateral bipolar (CSLB) inverter with the introduction of high-k BOX along with substrate bias for digital applications. The inverter shows a low noise margin (NM_L) and a high noise margin (NM_H) of 0.45 V and 0.37 V respectively when operated at 1.0 V.

Keywords

Silicon Germanium on Insulator; Symmetric lateral bipolar transistor; cut-off frequency; dielectric materials; Substrate Biasing.

1. Introduction

New challenges have emerged in VLSI/Semiconductor industry especially for digital and mixed signal circuits due to continuous effort to sustain the Moore's law. Non planar devices such as FinFETs and Silicon-on-Insulator (SOI) have limitations to the problems arising from further scaling particularly for low power applications.

Symmetric lateral bipolar on SOI seems to overcome the issues related to scaling in the niche extremely low power high frequency analog/mixed signal applications. This novel device has lower standby power consumption for digital circuits as demonstrated [1-7]. Some low power high frequency applications where symmetric lateral bipolar on SOI find itself as promising candidate are CBipolar, I^2L, I/O and clock driver circuits.

A Si homogenous CBipolar using symmetric lateral bipolar on SOI is calculated to have Standby power of 10nW with delay of around 2ns at V_{CC} = 0.8V [7]. They also projected that with heterojunction symmetric lateral bipolar on SOI, a CBipolar with reduced V_{CC} at 0.5V would further reduce the standby power dissipation upto 0.1pW and also reduce the active power dissipation.

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Despite being the densest circuit the main drawback of I^2L circuit with vertical bipolar is the speed which is limited to >200ps. Delay being scaled down to <10ps has been reported with use of symmetric lateral bipolar on SOI in I^2L circuits [7]. The report also suggests that with further scaling of the symmetric lateral bipolar, a power-delay product upto <10aJ is possible.

I/O and clock driver circuits require transistors to have high drive current capability. I/O circuit using CMOS have about 1mA/μm drive-current capability while I/O circuits using symmetric lateral bipolar on SOI approaching about 10mA/μm drive-current capability is reported [7]. Area and associated capacitances of I/O and clock driver circuits using symmetric lateral bipolar on SOI are reported to be much smaller compared to using CMOS. This means the circuits with symmetric lateral bipolar on SOI will have much lower power dissipation.

A better control over the performance parameters, gain and f_T, of this novel device was also achieved by introducing substrate biasing [8-9]. The device physical mechanism under substrate bias is discussed by J.-B. Yau et al in [8].

In this paper we investigate to optimize symmetric lateral bipolar on SiGe-on-Insulator (SiGe-OI) by varying the thickness of active device area, T_{SiGe}; BOX layer, T_{BOX} and using higher k-value of dielectric materials [10] in lieu of the traditional SiO_2 as BOX layer under zero biased/substrate biased condition. A uniform 0.3Ge mole fraction in Silicon is