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Priming and testing silicon patch-clamp neurochips

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We report on the systematic and automated priming and testing of silicon planar patch-clamp chips after their assembly in Plexiglas packages and sterilization in an air plasma reactor. We find that almost 90% of the chips are successfully primed by our automated setup, and have a shunt capacitance of between 10 pF and 30 pF. Blocked chips are mostly due to glue invasion in the well, and variability in the manual assembly process is responsible for the distribution in shunt capacitance value. Priming and testing time with our automated setup is less than 5 min per chip, which is compatible with the production of large series for use in electrophysiology experiments.

Introduction

Information is transported in the nervous system and processed in the brain in the shape of voltage peaks transmitted through networks of neuronal cells. Variations in potential are controlled in each cell by flows of ions from the cytosol to the extracellular fluid through its membrane by specialized proteins called ion channels. Ion channel electrophysiology is of fundamental importance to understand the basic functions of the brain and the nervous system, to study therapeutic strategies to alleviate its dysfunctions, and to screen new drug candidates. Among the techniques used to study ion channel function, patch-clamping [1,2] is the only one to truly give control of the cell inner potential, and is still considered the gold standard of electrophysiology. The technique employs a small-tipped glass pipette filled with electrochemically conductive physiological medium sealed to a patch of cell membrane by suction. An electrode immersed in the pipette clamps its voltage, and small currents resulting from ion channel activity across the membrane are recorded. While this technique has extremely high resolution, it is also slow and cumbersome as it requires expert manipulation and has very low yield. Leveraging microfabrication techniques, patch-clamp chips have been developed in the last decade [3,4], whereby the apex of the pipette is replaced by a micron-size aperture machined in a self-supported thin film that separates the culture medium from the physiological medium normally found inside the pipette. While quartz [5] and various polymer [6–9] chips have been reported, silicon patch-clamp chips [10–14] have the advantage of very mature and reliable fabrication processes. Silicon also has the inherent capability of on-chip amplification or analysis, which has been demonstrated with other neurochips [15,16]. On the other hand, the semi-conductive substrate creates electrical coupling between the two media baths, typically resulting in high shunt capacitance. This in turn limits the applicability of the technique to large cells having a larger membrane capacitance, or to the monitoring of relatively slow dynamics [17]. We have reported [18] the fabrication of silicon patch-clamp chips with a relatively low nominal shunt capacitance of 17 pF; this value still compares unfavorably with the typical 5 pF of glass pipettes and quartz patch-clamp chips, but it is compensated by a much lower access resistance (1 Mohm compared to typical 5–10 Mohm values for pipettes). The nominal 17 pF value however depends on the assembly process of the chip in a fluidic package. Due to variations of the gluing process, chips may have too large a capacitance. They may also be obstructed, or simply be too hydrophobic for the microscopic aperture to be primed, which makes them an open circuit unable to contact the membrane of the cell. In this paper, we report on a

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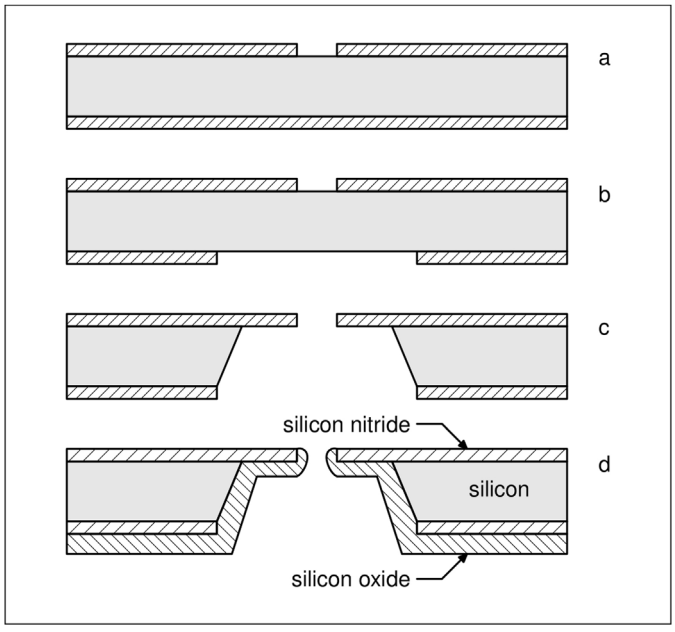

FIGURE 1

fabrication process of silicon patch-clamp chips. **(a)** A microscopic aperture is opened in a silicon nitride film and **(b)** a large square opening centered with the aperture is opened in the silicon nitride at the back. **(c)** Potassium hydroxide etches the silicon anisotropically in a pyramidal shape from the back till it reveals the unsupported silicon nitride film at the front. **(d)** A thick silicon oxide film is deposited at the back to passivate the well of the chip and round the edges of the aperture.

method to automatically treat the surface of chips, prime and test them in order to maximize the number of usable chips to electrophysiologists, as well as to gain insights to the shortcomings of the assembly process.

Chip fabrication

Silicon patch-clamp chips consist of a well excavated from the back of a silicon wafer to reveal a self-supported portion of an insulating membrane in which a micron size aperture is machined [18]. The insulating membrane is a composite of a silicon nitride film, with high mechanical strength and etch selectivity to silicon, and silicon dioxide, which is easier to functionalize for cell adhesion. The fabrication process is illustrated in Fig. 1. A 1 micron silicon nitride film is first coated on both sides of a 150 mm wafer by low-pressure chemical vapor deposition. A 4 micron microscopic aperture is etched in the silicon nitride at the front of the wafer, and then a square centered with the microscopic aperture is opened in the silicon nitride at the back of the wafer. The silicon bulk is then anisotropically etched in potassium hydroxide dioxide, creating a truncated pyramidal shape that ends at the silicon nitride layer in the front of the wafer, leaving it unsupported as seen on the scanning electron micrograph at the bottom left of Fig. 2. A 5.4 micron thick silicon oxide layer is deposited by plasma-enhanced chemical vapor deposition at the back of the wafer to passivate the silicon walls of the well and round the edges of the microscopic aperture; a very thin (100 nm) silicon oxide layer is finally coated at the front to facilitate cell adhesion. A cell positioned on the micron size aperture can be probed as in the patch-clamp method when bathed in a culture medium and when contacted through the aperture by an electrochemically conductive physiological medium. This requires the chip be assembled in a fluidic package containing the culture medium on top and allowing the physiological medium to be perfused from the bottom through tubes.

The chips fit in a recess of the Plexiglas package at the bottom of the culture chamber; a 1.5 mm circular hole at the bottom of the recess connects the back of the chip to subterranean channels. The gluing process is accomplished in two steps. First, using a manual glue dispenser (Oki DX 350, OK International http://www.okinternational.com/) under a binocular, a bead of Dow Corning RTV silicone 3140 glue is dispensed around the 1.5 mm hole at the bottom of the recess, and the chip is lowered in the recess with slight pressure. Then, a second bead of glue is dispensed around the edges of the chips to seal the silicon facets that have been revealed by singulation from the wafer in which they were fabricated and avoid shorts to the conductive bulk of the chip. The glue is allowed to cure for at least 24H; as the curing is moisture-activated, the glue quickly grows a solid 'skin' but in-depth curing takes time. While the second step is essential to obtain a high impedance chip, it is the first one that is critical for its impedance. Simple geometric considerations show that the shunt capacitance is dominated by the capacitance of the self-supported film and well plus that of the contact area between the bottom of the chip and the physiological medium. The former is precisely controlled by the micromachining of the chip and calculated to be 8 pF. Assuming that this area exactly corresponds to the 1.5 mm diameter of the hole connecting the chip to subterranean channels, the latter should be 8.6 pF. In practice, however, the contact area depends where exactly the glue is dispensed on the Plexiglas surface around the hole, and how it is squeezed when the chip is dropped in the recess. Too much glue or too much force applied on the chip, and the well might be invaded by glue, plugging the aperture; too little of either and the contact area may be much larger than desired – in extreme cases leading to leaks. Figure 3 shows an example of a chip dismounted from its package by soaking it in toluene for 15 min (the toluene softens the glue which releases from a soft bond with the Plexiglas package, but it remains firmly bonded to the silicon dioxide surface of the chip). The contours of the glue are clearly larger than the 1.5 mm diameter of the hole in the package, represented by a dotted line centered around the well. This correlates well with the measurement of a shunt capacitance of approximately 30 pF.

Testing setup

Probing the dynamic behavior of ion channels within a cell require as low a shunt capacitance and access resistance as possible, but also for the aperture to be properly primed with phosphate buffered saline (PBS) solution. In order to limit the number of faulty chips reaching electrophysiology laboratories, as well as obtain direct feedback on assembly parameters, chips are sterilized, primed and screened post-assembly. To sterilize the chips, they are treated in an air plasma (Harrick Basic Plasma Cleaner, http://www.harrickplasma.com). Importantly, this step also saturates the surface of the chips with hydroxyl groups, which renders them hydrophilic. Plastic surfaces however quickly revert to an hydrophobic state, so priming must occur shortly after sterilization. Chips impedance can be measured after priming with PBS. Their

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