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Density of interface states, excess capacitance and series resistance in the metal–insulator–semiconductor (MIS) solar cells

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Abstract

Dark and illuminatied current–voltage ($I-V$) characteristics of Al/SiO_x/p-Si metal–insulator–semiconductor (MIS) solar cells were measured at room temperature. In addition to capacitance–voltage ($C-V$) and conductance–voltage ($G-V$), characteristics are studied at a wide frequency range of 1 kHz–10 MHz. The dark $I-V$ characteristics showed non-ideal behavior with an ideal factor of 3.2. The density of interface states distribution profiles as a function of ($E_{ss}-E_v$) deduced from the $I-V$ measurements at room temperature for the MIS solar cells on the order of $\cong 10^{13}\,cm^{-2}\,eV^{-1}$. These interface states were responsible for the non-ideal behavior of $I-V$, $C-V$ and $G-V$ characteristics. Frequency dispersion in capacitance for MIS solar cells can be interpreted only in terms of interface states. The interface states can follow the a.c. signal and yield an excess capacitance, which depends on the relaxation time of interface states and the frequency of the a.c. signal. It was observed that the excess capacitance C_o caused by an interface state decreases with an increase of frequency. The capacitances characteristics of MIS solar cells are affected not only in interface states but also series resistance. Analysis of this data indicated that the high interface states and series resistance leads to lower values of open-circuit voltage, short-circuit current density, and fill factor. Experimental results show that the location of interface states and series resistance have a significant effect on $I-V$, $C-V$ and $G-V$ characteristics.

Keywords: Excess capacitance; Series resistance; Interface states; MIS solar cells; frequency dependent

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1. Introduction

The radiant energy of the sun is maintained by the nuclear transformation of chemical elements occurring in the sun's interior at a temperature of many million degrees. The resources of solar power are enormous but the solar energy is not presently used on a large scale because the expense of harnessing it is not economically viable. Solar power must supply the enormous and growing requirements of posterity within two centuries. Ground sources (such as coal, oil and uranium) as they near exhaustion will become more costly than solar power. Metal-thin insulating layer-semiconductor (MIS) type solar cells have turned out to be very attractive converters of sunlight into electricity. Therefore, MIS type solar cells have attracted much interest in the last few years [1–8]. In addition, metal–insulator–semiconductor (MIS) solar cells and MIS structures are very useful devices in studying semiconductor surface [9–24]. In this structure, metal and semiconductor remain separated by an insulating layer and there is a continuous distribution of surface states at the interface between the semiconductor and the insulator, characterized at a neutral level. There are two possible sources of error, which cause deviations of ideal behavior and must be taken into account. The characterization of interface states and series resistance in MIS solar cells and MIS structure have become a subject of very intensive research and reported in the literature for more than four decades [25–30]. The series resistance is an important parameter, which cause the electrical characteristics of MIS type solar cells and MIS structure [12,14,21,28,29]. Usually, the forward bias current–voltage ($I-V$) characteristics at high voltages deviate considerably from linearity due to the effect of parameters such as the R_s and N_{ss} [9,22,23,26,30].

A number of workers have suggested various ways of characterization of these interface states [11,17,26]. The relationship between the admittance (Y) of the interface state charging process above and the capacitance (C) and conductance (G) of MIS structure measured in the external circuit has been described and analyzed by Nicollian and Goetzberger [31,32]. They have observed that the capacitance decreases with increasing frequencies. These effects are obtained at low and intermediate frequencies $C-V$ and $G-V$ measurements. At low and intermediate frequencies the interface states can follow the a.c. signal and yield an excess capacitance (C_o). This model can be applied to the MIS solar cells. Interface states may affect the $C-V$ characteristics of MIS structures causing a bending of the $1/C^2-V$ as well as affecting the ideality factor. In general, a $C-V$ plot shows an increase in capacitance with an increase in forward bias. However, in recent years, an anomalous peak in forward $C-V$ characteristics attributed interface states and series resistance has been reported [19,21,23]. Ashok [28] derived an expression for the dependence of the ideality factor n on the interface parameter and applied voltage. Furthermore an empirical method for transforming non-linear $1/C^2$ vs. V plots into linear ones was given by Vasudev et al. [33], where a quantity called "excess capacitance" C_o, which causes a non-linearity in the reverse bias region, was introduced.