



SI-Studio, a layout generator of current mode circuits



Andrzej Handkiewicz*, Szymon Szczesny, Mariusz Naumowicz, Piotr Katarzyński, Michał Melosik, Paweł Śniatała, Marek Kropidłowski

Faculty of Computing, Chair of Computer Engineering, Poznań University of Technology, ul. Piotrowo 3a, Poznań, Poland

ARTICLE INFO

Article history:

Available online 10 December 2014

Keywords:

Design automation
Layout generation
Current mode circuits
SI filters
CMOS fabrication

ABSTRACT

This work is the answer to the so far unsolved problem of generation of integrated circuits topography for current mode circuits. Synthesis methods corresponding to already existing digital methods are proposed. Among others – the following has been shown: a digital adaptation of the row strategy for analog cell design, as well as performance control of the circuits with respect to chip area, power consumption and speed operation. The proposed algorithms are integrated with the already-existing tools for automatic layout generation of analog circuits with behavioral description at the beginning. At each stage of the synthesis process – an architecture description in the VHDL-AMS language was used, which so far has been not useful to synthesize. On the basis of the elaborated expert system, layouts of a filter pair and a filter bank were generated. The circuits were fabricated in TSMC 0.18 μm CMOS technology and results of measurements are presented. The elaborated approach makes a contribution to the realization of current mode circuits with complexity not achievable up to now.

© 2014 Elsevier Ltd. All rights reserved.

1. Introduction

Electronic design automation (EDA) for digital circuits is being strongly developed nowadays. The integrated circuits' market has been following the miniaturization trend for many years (Ziebart, 2007). In days of minimizing power consumption and chip area the usage of analog circuits expands to new branches of life. Therefore, despite all profits of digital circuits there is a lot of adaptations for analog networks because of their better power, area and speed properties. Realization of these goals allows to obtain complex electronic systems as portable devices (Fang, Huang, & Tseng, 2013). Current-mode analog circuits are especially interested with respect to these properties and to fabricate in standard digital CMOS process (Mak, Lam, Ng, Rachmuth, & Poon, 2010). Unfortunately the design process is much more complicated for analog circuits in comparison to digital ones (Kuo & Wu, 2014). The layout design stage seems to be the hardest one because of high risk of making mistakes and many physical, electrical and technological constraints. A designer has to spend long time to solve all these problems. Moreover, changing technology to a newer one requires rebuilding the whole circuit. Therefore

technology-independent of the analog circuits' design automation is a topical problem. Scientists look for synthesis methods, dedicated to analog circuits (Castro-Lopez, Guerra, Roca, & Fernandez, 2008), which could solve the problem of chip area minimization, being aware of geometric constraints and parasitic effects. Authors Castro-Lopez et al. (2008) propose a methodology for sizing AMS-circuits and put the problem into a block diagram, as a kind of an algorithm with few stages which can be easily used for creating computer tools to simplify designers' work. The layout floorplan is based on the Stockmeyer algorithm (Stockmeyer, 1983) and on the slicing style (Otten, 1982) with recursive division of the layout area into vertical and horizontal slices.

The placement task for analog circuits is one of the topics taken up by Yilmaz and Dündar (2009). The authors propose methods for global and local routing. This work is especially important from the analog circuit design automation point of view. The presented analog Layout Generator (ALG) offers the possibility of generating a single folded, merged, interdigitized and common centroid transistors, which are used to solve the mismatch problem.

Despite the fact that analog circuit design automation is a topical problem, there are not as many works and solutions which would offer new tools or methods as for digital circuits. All of the above reasons inspired the authors of this work to elaborate computer tools, which reduce the complexity of layout design of analog circuits to the level comparable with digital circuits' design. It is shown in the paper that design automation is achievable in the case of switched-current (SI) technique starting with behavioral

* Corresponding author.

E-mail addresses: Andrzej.Handkiewicz@put.poznan.pl (A. Handkiewicz), Szymon.Szczesny@put.poznan.pl (S. Szczesny), Mariusz.Naumowicz@put.poznan.pl (M. Naumowicz), Piotr.Katarzynski@put.poznan.pl (P. Katarzyński), Michal.Melosik@put.poznan.pl (M. Melosik), Pawel.Sniatala@put.poznan.pl (P. Śniatała), Marek.Kropidlowski@put.poznan.pl (M. Kropidłowski).

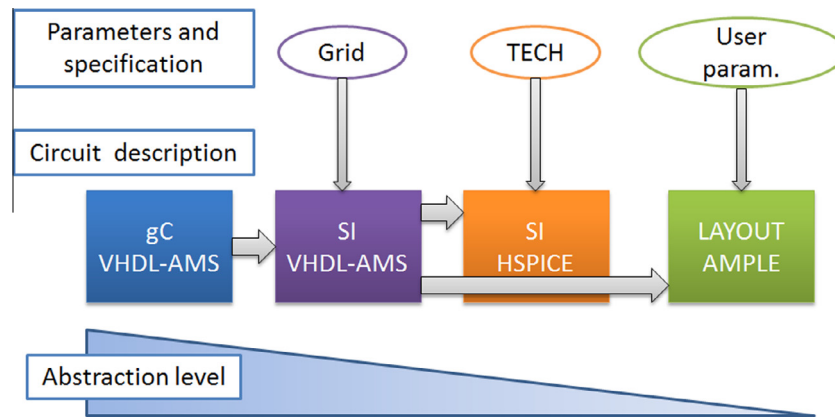


Fig. 1. Concept of system including main design stages, user's and technology parameters.

description and finishing with layout generation. In the obtained design strategy the following digital techniques for the synthesis of analog circuits architecture have been adopted: partitioning of architecture into blocks of standard cells, using the typical digital row strategy in designing a layout and a regular digital router. Presented methods offer power, area and speed control, and technology independent design, simultaneously making possible to obtain results at least as proper as the hitherto strategies bring.

The main foundations and goals of a CAD system for layout generation are formed in Section 2. Realization of the system and its verification scheme is presented in Section 3. Design focused on area, power and speed is presented in Section 4, in which the results of different designs are shown and compared. Section 5 shortly introduces computer tools created using the proposed methods. Section 6 presents in details a case of filter pair design, as an example of using the proposed methods. To corroborate the obtained results experimental circuits have been fabricated in the TSMC 0.18 μm technology. It is, at the same time, a case study of the first synthesis which was done for an analog SI circuit fully automatically designed from a description in the VHDL-AMS language. The language has been so far not useful to synthesize. As another confirmation of the efficiency of the methods – an analog filter bank circuit has been considered. It is probably the most complicated SI circuit which has been ever fabricated.

2. Foundations of a system of layout design automation

The current section elaborates on goals and constraints for the proposed strategy. Analog circuit design automation is obviously the main object, but parameterization and compatibility with existing tools and language standards are also important from the practical point of view. Therefore, a few additional goals are being defined in the beginning.

2.1. Aims, requirements and constraints

Design time and high risk of making mistakes are the most important determinants for the method elaborated on. There are two additional problems which the solution being offered needs to come up with: parameterization and technology independence. Taking into account all these expectations the following aims have been formed:

1. Final CAD system has to realize the last analog SI circuit design process step – drawing a layout of the SI circuit. Because SI circuits consist of integrators, memories, comparators, current mirrors, etc., such a system should be, first of all, able to draw these cells.

2. For the given functionality the SI circuits can possess different properties. Because it is easy to reduce power consumption and chip area or to increase the work speed by changing transistors lengths, it is worth to use such properties and offer the designer a tool which meets various design goals.
3. To ensure compatibility with the existing design tools and circuit description standards, the created system should cooperate with programs previously elaborated (Rudnicki, 2006) on one hand, and use the VHDL-AMS and HSPICE netlist description languages on the other.
4. Integrated circuits fabrication is an extremely expensive venture. Therefore, the designer should have a verification possibility, before sending the project to a foundry.
5. Integrated circuits are fabricated in a specific technology and it often appears a necessity to re-design a circuit to a different technology. To avoid the need of designing a circuit from the beginning – the strategy should offer technology independence.
6. It should be adaptable to different switched-current applications according to the idea of versatility.
7. Analog SI circuits are usually used for data pre-processing and thanks to analog-to-digital converters work together with the digital part of a mixed system. It is worth to notice that digital circuits are usually designed using the so-called row strategy (Clein, 2000). Its adaptation to the task of designing analog circuits would open new possibilities of designing complex mixed systems.

2.2. Data flow

Structure of the proposed ASIC design system is shown in Fig. 1. The design path has been divided into four different stages, in which the current circuit architecture is combined with a suitable language description. Additional information is included as parameters and specification. Some of the stages were already automated and the created CAD tools were presented in literature. The process begins with a gyrator-capacitor prototype circuit described in VHDL-AMS language. Such a description consists of capacitances and gyrators with their parameter values, connections between capacitors, as well as gyrators, and finally, of terminal port mapping. Such gC structure can be also automatically obtained (Handkiewicz et al., 2014; Katarzyński, Melosik, & Handkiewicz, 2013). The expert system described in these papers is based on the methods presented in (Handkiewicz, 1988, 1991; Handkiewicz, Katarzyński, Szczepny, Wencel, & Śniatała, 2012). Let us note that the gyrator-capacitor circuit, being lossless, possesses the low-sensitivity properties of transfer function magnitude with respect to circuit parameters, like LC ladder circuits.

Download English Version:

<https://daneshyari.com/en/article/10321872>

Download Persian Version:

<https://daneshyari.com/article/10321872>

[Daneshyari.com](https://daneshyari.com)