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Hardware implementation of optical flow constraint equation using FPGAs

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Abstract

This paper describes the hardware implementation of a high complexity algorithm to estimate the optical flow from image sequences in real time. Optical flow estimation from image sequences has been for several years a mathematical process carried out by general purpose processors in no real time. In this work, a specific architecture for this task has been developed and tested with simulators of hardware description languages. This architecture can estimate the optical flow in real time and can be constructed with FPGA or ASIC devices. This hardware has many applications in fields like object recognition, image segmentation, autonomous navigation, and security systems. The final system has been developed with hardware that combines FPGA technology and discrete FIFO memories.

Keywords: FPGA; Motion estimation; Optical flow; Image processing

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1. Introduction

The artificial vision is the main method of environment capture for further processing in artificial intelligence applications. In artificial vision two different and complementary aspects are taken into account. On one hand, the theoretic analysis of image processing methods oriented to extract information from scene, and, on the other hand, the availability of electronic circuits capable of carrying out those processing tasks with enough performance. The amount of information contained in images is very large, and to extract and to analyze that information by electronic means has a lot of applications. Until relatively few years ago, the technology only allowed us to process static images, but nowadays with the development of faster electronic devices and more complex processors, it is possible to extract information from image sequences.

The information contained in image sequences is larger than that contained in static images, since the former also provides information on the motion and the relative three-dimensional position of the objects. The extraction of that information not only requires better electronic devices, but also new ways of using them [1]. However, until now, satisfactory information extraction from image sequences in real time cannot be considered a goal fully achieved.

Usually image sequence processing is accomplished in high speed general purpose processors, but until now, the time involved to process image sequences in flows of 25 or 30 frames per second was very large. However, the use of new integrated circuits technologies, new smart algorithms, and new hardware design tools has made it possible to develop circuits to process image sequences in real time as previous stages in image analysis.

A key task to extract information from image sequences is to determine the movement of the objects in the scene. To do this, different algorithms have been proposed. Each author includes some improvements or new ways of calculating the movement of the objects in an image sequence. In most of the cases, it is necessary to obtain the optical flow of the image sequence. Optical flow is defined as the apparent motion of brightness pattern in an image sequence [22]. It can be considered as an approximation of motion field of each pixel in the image. Usually, optical flow estimation is carried out using spatio-temporal gradient algorithms [23,48,31,54]. These algorithms work by determining the spatial and temporal bright changes (gradients) of the image gray pattern, and estimating the optical flow from these parameters. This method is based on the fact that object movement produces changes in brightness.

The goal of this work is to design an optical flow estimator in real time for applications of motion estimation in image sequences. The optical flow estimator has been designed using the hardware description language VHDL to permit test and migration between technologies. The estimator has been simulated in a platform designed to test image sequences processing systems. Finally, it has been implemented with FPGAs to validate the results in real devices.

For the purpose of this work, real time means that the system can process video images at standard black and white TV rates. In digital terms, this rates can be defined as 256×256 pixel images in 256 levels of gray (8 bits) flowing at 60 images per second.