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Parameter variation aware hybrid TFET-CMOS based power gating technique with a temperature variation tolerant sleep mode

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ABSTRACT

In this work, we discuss the origin and temperature dependence of various mechanisms behind the flow of leakage current in two topologies of TFET – basic TFET and pocket doped TFET. It is shown that the leakage current of pocket doped TFET shows relatively less variations with change in temperature when compared with MOSFET and basic TFET, and hence they can be deployed in low voltage temperature variation prone applications. But, this advantage of pocket-doped TFET is overshadowed by the huge sensitivity of its ON-state current towards variations in doping concentration at the tunnel junction. Hence, the fabrication of the TFET based circuits requires a negotiation with the yield and cost of the fabrication process. In order to mitigate this issue, we propose a hybrid TFET-CMOS based power gating technique. The hybrid technique utilizes a minimum number of TFETs to reduce the sleep mode leakage current, while enabling a temperature variation tolerant sleep mode at a supply voltage of 0.6 V.

1. Introduction

Dennard's scaling laws have largely benefited a class of applications that are computationally intensive in nature. This is because the dimension miniaturization has lead to the efficient realization of complex functions without incurring a significant area overhead. The voltage down-scaling aspect of Dennard's scaling has brought down the supply voltage to near about 1 V and has opened up a new world of mobile devices. Unlike the dimension down-scaling, the voltage down-scaling has ceased after 1 V. This is because the reduction of the supply voltage requires a simultaneous reduction of the threshold voltage, but the leakage current of conventional MOSFET increases with the down-scaling of its threshold voltage. Moreover, conventional MOSFETs are based on the principle of thermal injection of carriers across the potential barrier, whose height in turn is modulated by the gate voltage such that in OFF-state the barrier is sufficiently high to suppress the thermal injection of carriers. But, as carriers gain thermal energy due to increase in temperature, thermal injection is no longer suppressed and relatively more number of carriers can cross the energy barrier and constitute the sub-threshold leakage current. Such a rise in the leakage current can trigger a serious reliability issue known as thermal runaway [1]. Hence, there are two main issues with conventional MOSFETs: (1) rise in leakage current with reduction of threshold voltage and (2) temperature variation sensitive OFF-state.

Band-to-Band Tunneling (BTBT) of electrons across a reverse biased gated *PN* junction is one of the promising idea that can reduce the dependence of sub-threshold leakage current on temperature and threshold voltage. Transistors working on this idea are known as Tunnel FETs (TFETs) [2]. This novel device features three lucrative characteristics for low-voltage circuits: (1) less-than 60 mV/dec *point* sub-threshold slope ($[dI_d/dV_{gs}]^{-1}$); (2) threshold voltage down-scaling without a significant increase in leakage current; (3) OFF-state current limited by generation and gate oxide tunneling current only. Attempts are being made to align it with mainstream circuit design. Unfortunately, these advantages are also accompanied with the following drawbacks: (1) low ON-state current; (2) greater-than 60 mV/dec *average* sub-threshold slope; (3) realization of TFET based circuits; (4) fabrication of structures with improved performance; (5) large sensitivity towards variations in process parameters. A large number of topologies have been proposed in order to address the issues with the ON-state current and sub-threshold slope [3–7]. In any topology of tunnel FET, the process of band-to-band tunneling of electrons is initiated by the dual effects of band bending and band lowering such that the empty states in the conduction band and the filled states in the valence band are aligned. Although the combined effect of band bending and band lowering eventually results in band-to-band tunneling of electrons, but the way in which bending and lowering are achieved results in significant leakage current also. In this paper we discuss the change in mechanism behind leakage with change in doping across tunnel junction. The discussion is supported with

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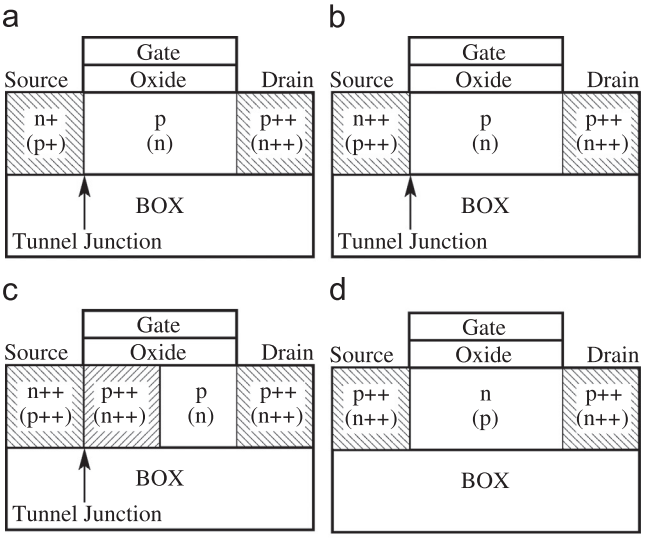
a comparative analysis of three different topologies of TFET: silicon based basic TFET employing n^+p junction, silicon based basic TFET employing $n^{++}p$ junction and silicon based pocket doped TFET employing $n^{++}p^{++}$ junction, each showing a different level of band bending. Comparison is also made with a MOSFET of a similar threshold voltage. Results and discussions presented henceforth are based on the TCAD simulations performed using ATLAS device simulator [8] with the following physical models: non-local band-to-band tunneling, SRH with concentration dependent lifetime, non-local trap-assisted tunneling, field and concentration dependent mobility and band-gap narrowing due to heavy doping. The band-to-band tunneling model used in simulations is calibrated against the experimental work reported in [9], details of which are given in Fig. 2.

Although TFETs feature lucrative characteristics for low power circuits, but its circuit interaction is still a lagging area. This is because of two main issues associated with TFETs: (1) electrical characteristics of TFETs are susceptible towards variations in process parameters [10–12], which in turn can decrease the yield of the fabrication process; (2) various promising topologies of TFET are non-conventional structures employing low band-gap material (s) [13,7]. Fabrication of such structures can escalate the cost of the fabrication process. In order to address the yield and cost related issues, we propose a hybrid TFET-CMOS circuit topology that utilizes a minimum number of tunnel FETs to reduce the leakage current flowing through a circuit block.

The rest of the paper is organized as follows. Section 2 discusses various mechanisms behind the flow of leakage current in TFETs. Temperature dependence of the leakage current of the TFET is compared with that of the MOSFET in the latter part of the section. Section 3 begins with the study of impact of parameter variations on the performance of C-TFET based circuits and ends with a discussion on hybrid TFET-CMOS based circuit topology. Finally, we conclude our work in Section 4.



Device Parameters	
T_{Oxide}, EOT	2nm, 0.35nm
T_{Body} (Silicon)	10nm
T_{BOX}	50nm
L_g, L_{Pkt}, W	45nm, 6nm, 1μm
n^{++}/p^{++} (except pocket)	10^{20}/cc
n^{++}/p^{++} (pocket)	3.5×10^{19}/cc
n^+/p^+	10^{18}/cc
n/p (TFET and low-V_{th} MOSFET)	10^{15}/cc
n/p (High-V_{th} MOSFET)	10^{17}/cc

Fig. 1. Various P(N)-FETs considered in this work. Structures (a) and (b) are basic TFETs, while structure (c) is a pocket (pkt) doped TFET. Structure (d) is a P(N)-MOSFET. Note that the doping and length of pocket are optimized such that it remains fully depleted at all voltages.

2. Leakage current of tunnel FETs

The analytical model of band-to-band tunneling suggests that the ON-state current of tunnel FET can be increased by reducing the bandgap and increasing the electric field across the tunnel junction [2,14]. Such a change in the ON-state current is also accompanied with a rise in the leakage current. In this section, we investigate the mechanism behind the leakage through the tunnel junction in P-TFETs as the nature of the junction is changed from n^+p to $n^{++}p$ to $n^{++}p^{++}$. Tunnel FETs employing $n^{++}p^{++}$ junction are known as pocket doped tunnel FETs [3], while those employing n^+p or $n^{++}p$ junction are termed as basic tunnel FET in the rest of the paper. These structures are shown in Fig. 1.

2.1. Effect of junction doping on origin and temperature dependence of leakage current

Threshold voltage and the voltage at onset of tunneling divides the transfer characteristics of any tunnel FET into three regions (see Fig. 3): (1) region showing a weak modulation of the tunnel width; (2) region showing a strong modulation of the tunnel width and (3) trap-assisted generation dominant region. Trap-assisted generation current flowing across any silicon based reverse biased junction is governed by two competing mechanisms: (1) phonon assisted generation via deep level traps (SRH) [15] and (2) generation due to trap-assisted tunneling (TAT) [16]. The electric field and doping concentration at the tunnel junction decide the relative dominance of these mechanisms.

PN junction theory quantifies the leakage current due to trap-assisted generation via deep level traps by the following equation

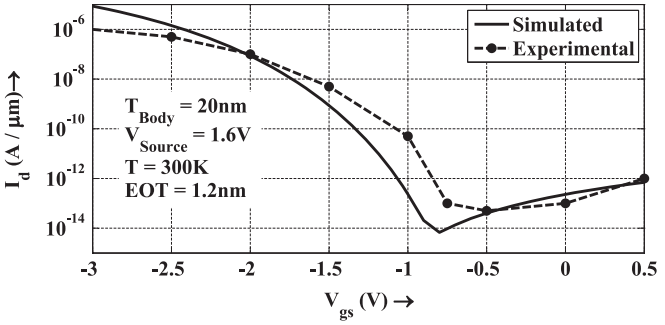


Fig. 2. Calibration of band-to-band tunneling model with the experimental results given in [9]. Note that the difference in the subthreshold region is mainly because of traps generated in device due to damage in SOI layer as reported in the experimental work.

[18,15]:

$$I_{SRH}=\frac{qA_jW_j}{2\dfrac{\tau_0}{\left(1+\dfrac{N_d}{N_{d0}}\right)}}n_i=\frac{qA_jW_j}{2\dfrac{\tau_0}{\left(1+\dfrac{N_d}{N_{d0}}\right)}}(\beta T^{3/2}e^{-E_g/2kT}) \quad (1)$$

$$I_{TAT}=\frac{qA_jW_j}{2\dfrac{\tau_0}{\left(1+\dfrac{N_d}{N_{d0}}\right)^{(1+\Gamma)}}}(\beta T^{3/2}e^{-E_g/2kT}) \quad (2)$$

where A_j is the junction area, n_i is the intrinsic carrier concentration, W_j is the width of the depletion region, β is the material