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Non-destructive high-resolution characterization of buried interfaces for advanced interconnect and packaging architectures: Experiments and modeling

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Abstract

Characterization of buried interfaces in advanced interconnect and packaging structures is a critical challenge as complementary metal-oxide-semiconductor (CMOS) devices are scaled and as novel packaging and interconnect concepts and materials such as three-dimensional (3-D) circuits, and ultra-low dielectric constant insulators are developed. Critical information that needs to be obtained from such inspection includes detection of unbonded bumps in flip-chip packages; missing interconnections in bonded wafers and presence of delaminations in interconnect layers. In this paper, we discuss in detail our experimental and theoretical investigation of different non-destructive characterization techniques namely acoustic imaging, infra-red imaging and transient thermal microscopy to analyze and quantify the quality of buried interfaces. The imaging resolution is shown to critically depend on the material thickness through which the incident probe beam has to propagate to form the images. Defects in buried interfaces such as voids in bonded wafers appear as regions of bright contrast in acoustic imaging due to large acoustic impedance mismatch at the voids. In the case of transient thermal microscopy, unbonded areas will lead to non-uniform temperature distribution at the surface of the substrate when the sample is rapidly heated with a flash lamp. The localized temperature rise at the defect and its temporal evolution can be related in turn to the defect size. We discuss capabilities and limitations of the different techniques for inspection of buried interfaces with an emphasis on characterizing bonded interfaces for 3-D integrated circuits. It is shown that acoustic imaging with single spherical lens is better suited to study bond quality compared to thermal microscopy due to its better detection capabilities. Infra-red imaging was found to be unsuitable for investigation of bonded interfaces in wafers containing multiple layers of metallization.

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1. Introduction

Non-destructive characterization of buried interfaces is very important to successfully invent and develop novel interconnect and packaging technologies. For example, three-dimensional integration is predicted to be a key enabler for continued device scaling and for heterogeneous integration of multi-functional devices [1]. Such 3-D circuits utilize building devices in the third dimension and typically require process steps such as wafer (/die) bonding, thinning, and also through-silicon vias for power and signal delivery [2,3]. It is, therefore, extremely important to develop novel characterization techniques that are non-destructive and at the same time enable high-resolution inspection of various interfaces in the device. An example of such an architecture is illustrated in Fig. 1 and the various interfaces of concern are marked. The two substrates bonded to each other could be made of silicon or silicon bonded to other materials for heterogeneous integration applications. The *bonding interface* between the two wafers is one of the most critical interfaces that need to be studied since any unbonded regions can cause catastrophic failures and yield losses. It is worth noting that the bond interface is typically buried anywhere from a few to several hundred microns beneath the surface of the wafer depending on post-processing conditions after bonding.

In this paper, we investigate different non-destructive characterization methods namely acoustic microscopy, infra-red (IR) imaging and transient thermal microscopy to study bonded interfaces as a model example of a buried interface in terms of resolution and contrast. It is shown that both acoustic microscopy with single spherical lens and pulsed thermal microscopy can image defects in bonded interfaces effectively. Acoustic imaging offers better resolution for imaging interior layers even though both techniques offer similar resolution for imaging surface features.

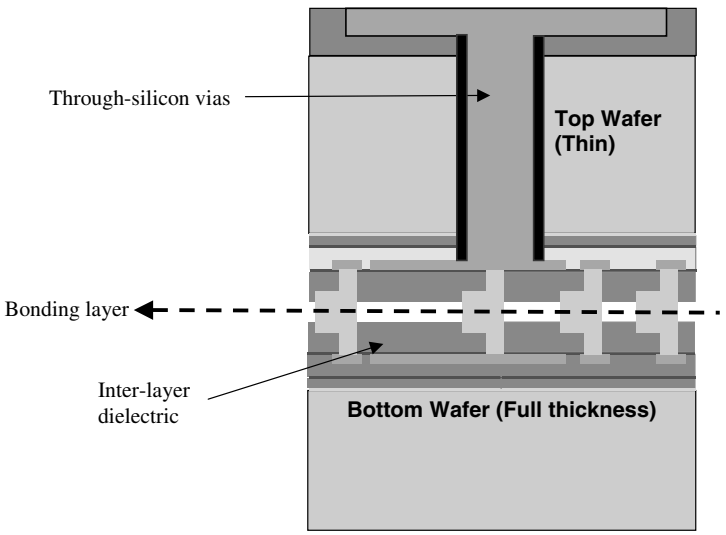

Fig. 1. Schematic of a three-dimensional integrated circuit. Two wafers are bonded together with a high density of interconnections in between. The two wafers could be made of identical materials (e.g., Si) or dissimilar materials for heterogeneous integration of multi-functional devices. Characterization of the bonding layer uniformity is critical to enable electrical connections between the two devices. Interfaces of concern are marked in the figure.